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Precise linear signal generation with nonideal components and deterministic dynamic element matching

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Precise linear signal generation with nonideal components and deterministic dynamic element matching

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Signatures have been redacted for privacy

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ABSTRACT

A dynamic element matching (DEM) approach to ADC testing is introduced. Two variants of this methods are introduced and compared; a deterministic DEM method and a random DEM method. With both variants, a highly non-ideal DAC is used to generate an excitation for a DUT that has effective linearity that far exceeds that of the DAC. Simulation results show that both methods can be used for testing of ADCs. The deterministic DEM (DDEM) offers potential for a substantial reduction in the number of samples when compared with a random DEM approach with the same measurement accuracy. It is shown that the concept of using DEM for signal generation in a test environment finds applications well-beyond ADC testing. The DDEM approach offers potential for use in both production test and BIST environments.

CHAPTER 1: GENERAL INTRODUCTION

In this chapter the thesis context, stating the objective behind this work will be first explained. Then other researchers work will we analyzed to give a complete view of the work that is being and was done in this area.

1. An introduction to mixed-signal integrated circuits testing

A mixed-signal circuit can be defined as a circuit consisting of both digital and analog elements [1]. The most common and widely use mixed-signal circuits are digital to analog converters (DACs) and analog to digital converters (ADCs). Data converters are so widely used because they serve as the interface between digital logic and the analog or physical world.

Mixed-signal circuits need to be tested to assure that the behavior obtained once fabricated meets specifications. Many factors can cause a circuit to fail to meet specifications. During the fabrication process catastrophic defects can occur, such as unwanted short or open circuit. Catastrophic errors are usually easy to find during testing. A more challenging testing problem occurs when the error is more subtle and only affects a few specifications of the circuit but not its functionality. For example, if during design sufficient area is not allocated to matching critical capacitors, a significant percentage of functional circuits may not meet required performance specifications. A doping error during fabrication could also introduce large DC offsets or distortion that could cause a circuit to fail to meet specifications. Thus, most mixed-signal circuits need to be intensively tested in order to assure compliance with desired specifications.

Testing is often an expensive process that does not add functionality to the circuit, it just provides a measure of quality. Quality of the product is improved if we can assure through testing that no faulty parts are going to be sent to the customer. Having that in mind, testing adds value to the final products since it helps assure quality of the product supplied to the costumer.

1.1. Test equipment

Automated test equipment (ATE) is available from a number of different vendors. ATE often consists of three major components; a workstation, the mainframe and the test head. The workstation is the interface between the tester and the test engineer. Different testing routines can be programmed using the workstation and the results of the test can be communicated to the test engineer via the workstation. The workstation is also used for maintaining the tester. The mainframe consists of the tester hardware used to test a circuit. It is complied of different types of sources, probes and other components needed to excite the circuit under test and obtain the resultant test data. This hardware is controlled by the software running on the workstation. Some circuits have critical input signals whose sources need to be closer to the circuit under test. These critical circuits are placed on the test head.

Other equipment is needed for testing beyond the ATE. This other equipment includes wafer probers, forced temperature systems, handlers, etc. This equipment is expensive (usually more than $ 2,000,000 dollars and rising) and requires costly maintenance on regular basis to obtain reliable test results.

1.2. Mixed-signal testing challenges

The mixed-signal testing task presents several challenges which will be discussed in this section. We will mention just few of them, such as time to market, accuracy and the economics related to testing.

Time to market is an important issue since many product needs to be on the market fast to be competitive in the market. Testing is often a challenging task. To address this task, the test engineer and the design engineer need to work together so that when the silicon is available, a test setup is also available. Sometimes even this is not good enough since some problems can only be address once the silicon is back. In these cases the tester and the testing software may need to be developed in conjunction with measured test results.

Another challenge is the test accuracy. External factors such as noise, test setup, tester calibration and capacitive or inductive connections can compromise the accuracy of a test. All these factors need to be taken into account to obtain accurate measurements.

Testing economics is a big factor. In production test time is money; one second of test time often cost from 3 to 5 cents on production testers. With transistor sizes shrinking, the cost of adding functionality to many circuits is really low, but the testing costs often increase (more functionality means more complex testing). So the tests not only need to be accurate, but they also need to be done as fast as possible. This generates a conflict between accuracy and time that the test engineer needs to address when a testing scheme is developed.

1.3. Design for test

Any design methodology or circuits that make a product more testable can be categorized as design for test (DfT) [1]. There are two identified approaches to DfT, the standardized approach and the ad hoc approach.

The standardized DfT approach is usually structured and hence sometimes does not give all the results needed, it also sometimes add extra circuitry that can potentially affect the performance of the mixed-signal circuits. Although this approach is popular in digital testing, it is not widely used in mixed-signal circuits where added parasitics needed for the DfT capability can cause a circuit to fail to meet its expected behavior. One example is the IEEE 1149.4 mixed-signal test standard; this standard was developed to give a solution for mixed-signal fault testing but it can only be use with low frequencies circuits since the boundary scan added to the circuit will adversely affect the performance at high frequencies. This standard covers only a small portion of the requirements needed for testing. The standard does, however, allow ad hoc testing schemes within a circuit compliant to the standard.

Ad hoc schemes are often more circuit focused. A technique that works for a specific circuit probably will not work for another unless some modifications are done. Built-in-self-test (BIST) is one variation of an ad-hoc scheme. With BIST, the idea is that the ATE provides only basic signals (a power supply and/or a clock) while the circuits test themselves and provides a status or a fault signal to the ATE or provide a bit stream with the measurement results.

In the past, design engineers did not want to add testability features to silicon, since they add to the die size, the design effort and the cost. This behavior was supported by

managers and customers but now a change is in progress. Currently design engineers, managers and customers have realized some of the advantages of DfT such as an overall reduction in production cost.

A BIST approach can be part of a control loop that calibrates the circuit, improving its behavior and increasing the yield. It can also give the costumer the chance to test the circuit so that it can be monitored in the environment in which it is used. Other benefit from using BIST schemes is that the ATE used for testing can often be less accurate and less complex and hence less expensive.

We can summarize saying that DfT (including BIST) often lowers test costs through a reduction in test time and through the use of less expensive equipment. Calibration schemes can provide added value to the product.

2. ADC static linearity testing

The DC ADC transfer characteristics map a continuous input range to different code outputs depending on the input voltage value. Static characteristic of an ADC are determined from the transition points between adjacent codes and static linearity testing generally involves determining the locations of these transition points based upon measure data. Ideally the transitions from one code to the next are fixed and equally separated, but reality shows that the transitions differ from their ideal value and are affected by noise in the transitions. Since noise is a random variable, the ADC transition characteristics are statistical in nature rather than deterministic.

For input voltages that are close to but not equal to a transition level, if either the ADC or input signal noise is big enough, it can make the ADC give an erroneous conversion result. Because the ADC circuit generates random noise, the decision (transition) levels represent probable places were the transitions from one code to another occur.

If we plot the cumulative codes from a typical ADC vs. DC input levels, we will see not a linear relationship. More noise gives more variation from one code to the next one.

Because of the statistical characteristics we have just mention, the measurement of these transition points is not an easy task and it generally required a large number of measurements to achieve a reliable estimate of the actual value. This, of course, takes effort

and more importantly time. It has been stated before that tester time is money, so we will concentrate in developing approaches that give acceptable code edge accuracy in reasonable time.

One of the most used methods for ADC static linearity testing is the linear ramp histogram approach. In this approach, a highly linear ramp sources as the input to the ADC. The rise time of the ramp is slow enough so that each code is hit several times. The number of hits per code is proportional to the code width and the running sums are indicators of the linearity.

The number of occurrences are plot on a histogram where ideally each code should have the same number of hits. In this method we have assumed that the ramp is perfectly linear or at least that it is sufficiently linear for testing the ADC under test. The generation of a sufficiently linear ramp is not a trivial requirement when the ADC resolution is high.

To assure that all codes are hit, the input ramp range is bigger than the ADC range. This causes the first and last codes to be hit a lot more times that the others. These two code totals are eliminated from the histogram prior to any calculations of linearity parameters. The static performance of the ADC, i.e. INL and DNL, can be easily determined through straight forward calculations based upon code totals as will be shown in following chapters.

3. BIST approaches to ADC testing

During the past years lots of works have been published in the BIST area and some has been focused on ADC testing since the ADC is one of the most important and complex mixed-signal circuit available. In this section some of these works will be reviewed in order to put this thesis in context with other researchers work.

J. Wang; E. Sanchez-Sinencio and F. Maloberti report a very linear ramp generator in [2], but the linearity of these generators is only good to test up to 14-bit ADCs according to their simulations results. Although the circuits were fabricated, the experimental results are not shown in this work, so no conclusion can be draw about the actual ramp linearity. A similar approach was followed by S. Bernard, F. Azais, Y. Bertrand and M. Renovell [3]. They add a control loop to the ramp generator used to realize a triangular wave, but even with feedback the ramp linearity is at best 15-bit linear based on simulation results. This

allows testing up to 12-bit ADCs. In [4] B. Provost and E. Sanchez-Sinencio presented three different ways to generate on-chip ramps. All of them use an adaptive system to adjust the ramp slope. Although simulation results suggested that these 15 bit linear ramps can be generated, measurement results are no better than 11 bit linearity. In the paper they address some problems that can lead to this behavior including offset, matching issues and the finite output impedance of the current source, but they claim also to take care of those errors during the design process. Later when the measurement results are shown, no conclusion is draw about the difference between the expected linearity and the measured results.

Other authors are not comfortable with the ramp generation since they want to avoid the analog circuit overhead. Some have generated single or multiple tones using bit streams generated using ΣΔ modulators. Two different generators are reported in [5] by B. Dufort and G. W. Roberts. M. F. Toner and G. W. Roberts use this generator to measure the frequency response, harmonic distortion and intermodulation distortion on ADCs in [6]. They give experimental results indicating that this method provides results comparable to those obtained by using a regular FFT but with less computational effort. Previous work only refers to ΣΔ ADCs, and hence is architecture dependent.

A different approach was followed by K. Arabi and B. Kaminska [7]. In this work they did not use test stimuli. Their idea is to make the circuit oscillate and then by measuring the oscillation frequencies they can characterize the ADC. They claim the test scheme is ADC architecture independent but it is not clear how the control loop affects the system and how some reference voltages are generated. The show results are from measurements on two commercial 8-bit ADCs.

Other works are focused on reduced circuit processing capabilities, memory and hence circuit overhead associated with the on-chip calculation of the ADC characteristics. In [8], F. Azaïz, S. Bernard, Y. Bertrand and M. Renovell proposed different modifications to make the histogram method more suitable for BIST solutions by minimizing overhead circuitry. However the reduction of the overhead circuitry was obtained at the expense of an increase in the testing time. R. de Vries, T. Zwemstra, E.M.J.G. Bruls, P.P.L. Regtien in [9] presented a way improve the processing of the data, but in this case they are still relying on a highly linear input to the ADC.

As can be observed, all these works faced the same problem and that is the ADC input generation. Methods of reducing overhead in the processing are not useful if the data obtained is not valid because of insufficient linearity in the input. Thus, to assure that the input signal is good enough, the ADC resolution of the device under test must be moderate and at most 12 bits if prior art is used for generating a BIST environment.

A new way to achieve analog and mixed-signal BIST has been recently proposed. The basic idea is to dramatically reduce the accuracy requirements on the signal generator and then use system and signal processing techniques to accurately characterize and test the DUT. The method is explained and experimental results are shown in [10] by Le Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. L. Geiger. The concept is also analyzed in details in [11] by K. Parthasarathy, T. Kuyel, D. Price, Le Jin, D. Chen and R. L. Geiger.

In this thesis we present a novel way to generate a input signal with a very high effective linearity; using new dynamic element matching (DEM) techniques along with low accuracy DACs to achieve very high accuracy in the testing of high resolution ADCs. The silicon area used for these DACs will be very small making them viable candidates for practical utilization in production BIST environments.

4. Dynamic element matching

The dynamic element matching (DEM) technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average, the element values are nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated in some applications.

The DEM method was used by H. T. Jensen and I. Galton [12] [13] to improve the effective specifications of linearity performance of DACs by randomly rearranging the 1-bit DAC components or some of the multi-bit DACs components. They demonstrated that DEM can be used to appreciably improve the SFDR performance of moderately low-linearity DACs [12]. This is because the randomizing effect of DEM spreads the errors in the DAC over a wide spectrum so that higher SFDR becomes possible.

Other researchers use DEM in Delta-Sigma Converters. R. Adams, K. Q. Nguyen and K. Sweetland applied DEM on an oversampling DAC where they used noise shaped scramblers to achieve high SNR [14]. Z. Li and T. S. Fiez have studied different DEM algorithms in [15]. A new algorithm was introduced and analyzed in [16] by R. T. Baird and T. S. Fiez. This algorithm has no scrambler and the switching sequence depends on the input. Thus, in order to have good performance when applied to a ΣΔ DAC, random noise is added to the input so that the behavior is random. A ΣΔ DAC is implemented using a new algorithm in the work by R. E. Radke, A. Eshraghi and T. S. Fiez in [17], here the first decision on the algorithm to pick the elements on the DAC is random.

It is noted that all previous works on DEM require a "random" choice of matching critical elements, which implies that a scrambler or randomizer needs to be added to the circuit. Further, although these DEM approaches obtain good linearity specifications, they all require measurements over very long periods of time and essentially all have poorlinearity performance over short time intervals. This seriously limits where existing DEM strategies can be adopted.

5. Thesis motivation and organization

As was mention in previous sections, the ADC is one of the most widely used mixed-signal circuits. It is also a challenging circuit to test, particularly in view of the observation that resolution and speed keep moving higher. A possible solution to the ADC testing problem is to adopt the BIST approach. This method adds value to the circuit since it can now be tested by the costumer (if needed) and can also have some calibration features.

The biggest problem with existing BIST methods for testing ADCs with resolution higher than 12 bits is that of input signal generation. Our approach faces this challenge by using DEM in a poor (and hence small area) DAC which is used to generate a highly linear input to the ADC.

A paper published in Proceedings of the 2002 IEEE Midwest Symposium on Circuits and Systems is shown in Chapter 2. In this first work the concept of ADC testing using a DEM DAC is proven for low resolution ADCs. In this work the DAC elements were chosen randomly.

In Chapter 3, a paper introducing a new deterministic DEM algorithm is presented. This new algorithm is compared to the one used in Chapter 2. This is a paper that was published in Proceedings of the 2003 IEEE International Symposium on Circuits and Systems.

Chapter 4 and Chapter 5 are drafts of papers to be submitted to the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. The thermometer coded current steering DAC using the deterministic DEM (DDEM) is presented in Chapter 4. It is shown through simulation that this method can accurately characterized 16-bits ADCs. In Chapter 5 a new simpler DAC architecture is presented and characterized. The results obtained are similar to the ones shown in Chapter 4.

Finally in Chapter 6, some general conclusions and future work in this area are stated.

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CHAPTER 2: A DYNAMIC ELEMENT MATCHING APPROACH TO ADC TESTING

A paper published in Proceedings of the 2002 IEEE Midwest Symposium on Circuits and Systems

Beatriz Olleta, Degang Chen and Randall Geiger

Abstract

A dynamic element matching approach to ADC testing is presented. With this technique a highly nonideal DAC is used to generate an excitation for the DUT. Dynamic element matching is used to create a statically precise excitation from imprecise components. Simulation results show this approach can be used to accurately measure the performance of an ADC. This technique offers potential for use in both production test and BIST environments.

1. Introduction

Testing analog-to-digital converters (ADC) is a non-trivial task since an accurate input is needed. This input is typically generated by a digital-to-analog converter (DAC) with higher resolution than the device under test (DUT). In other words, the real challenge is designing the circuit to test the part, since it needs to have higher resolution and linearity than the DUT. This approach is not suitable for BIST applications since the DAC needs more silicon area than the ADC to be tested.

It is known that dynamic element matching (DEM) can be used to generate analog signals with high SFDR using a moderately low resolution digital-to-analog converters (DAC)[1]. This becomes possible due to this technique's decoupling of the DAC noise from the DAC input. In [1], it was shown that in a DAC with static errors, performance can be improved using randomization DEM. This characteristic of the dynamic element matching technique makes it a suitable candidate for generating the input of a DUT using a

not-so-accurate DAC. The focus of this work is to use a low accuracy DAC with DEM to characterize an ADC with higher accuracy.

In the proposed scheme, the DAC will have more bits than the ADC but is not ideal and has some static errors caused by mismatches. Static mismatch errors can be caused by process variations and result in a nonlinear transformation in the DAC, called integral nonlinearity (INL), which degrades the DAC performance. Similar mismatches in an ADC contribute towards its INL. Although any number of ADC performance parameters may be characterized, INL will be used to test the proposed scheme.

This paper is organized as follow. Section 2 explains how the ADC is implemented and how the INL is calculated. Dynamic element matching method is explained in Section 3. Section 4 gives details about the random DAC, while in Section 5 some simulation results are shown and discussed. The summary is in Section 6.

2. ADC model and INL calculation

To test our idea, a flash ADC is going to be characterized through the INL measurement. A simple implementation of a flash ADC is shown in Figure 1.

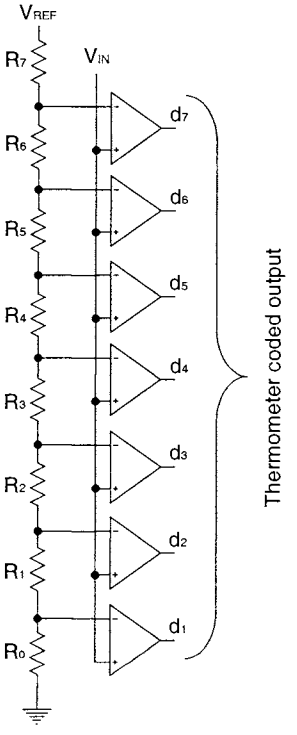

Figure 1: A 3-bit flash ADC.

The input signal in to a flash converter is fed to the comparators in parallel. Each comparator is also connected to a resistor string, as shown in Figure 1. The output of the comparator is set to one if the input value is bigger than the voltage of the resistor string. The output code obtained is called thermometer code. Resistor mismatch and comparator errors are the two primary sources of static errors contributing towards the INL of the ADC. For the purposes of this work, comparator mismatches are ignored and only the static error caused by resistor mismatches is modeled.

There are several alternative but similar definitions of INL of an ADC. The endpoint fit line method was picked for this work. In this definition, the INL, as given in (1), is defined to be the maximum deviation of the ADC's transfer curve from the endpoint fit line. With this definition, the INL of an ideal ADC is 0.5 LSB.

$$INL = \max\left(\left|\frac{V_o - V_{FITLINE}}{V_{LSB}}\right|\right) \quad (1)$$

An example with a non-ideal ADC transfer curve and its corresponding fit line is shown in Figure 2. It is a 3-bit flash ADC with a voltage reference equal to 2V.

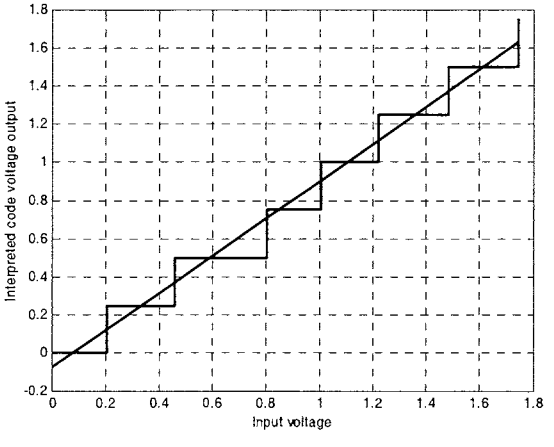

Figure 2: A nonideal ADC transfer curve and its endpoint fit line.

As can be seen in Figure 2, the INL has maximum values in the transition points when the output changes from one code to the next one. These are the points that need to be measured for characterizing the ADC under test.

3. Dynamic element matching

Element matching errors are inevitable due to inherent process variations. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The dynamic element matching technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average the element values are nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated.

Existing DEM structures are used in real-time circuits, making difficult to fully exploit DEM potential. Our approach is different since the DEM is not in the DUT but in the signal generator, eliminating the real-time concern when using DEM.

4. A DAC with dynamic element matching

In order to construct a DAC with dynamic element matching two different approaches can be found in the literature [1- 2]. One is the partial randomization DEM. The other is the so called full randomization DEM. This latter technique is used in this work and will be explained next along with some modifications.

The full randomization DEM will be explained using a 3-bit current mode thermometer-coded DAC as an example as shown in Figure 3.

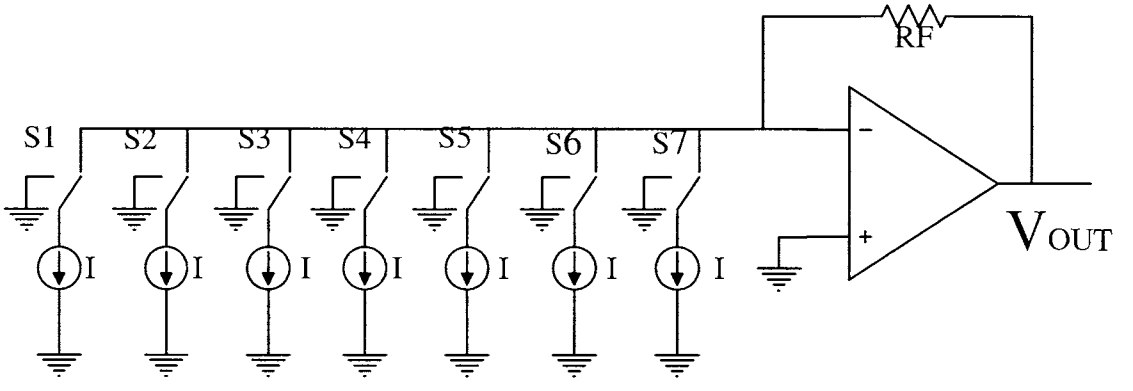

Figure 3: A 3-bit current mode thermometer-code DAC.

In this case when all the switches are connected to ground the output corresponds to the digital word zero. To have the output voltage for a digital one, one switch needs to be connected to the negative input of the Operational Amplifier (opamp). The idea is to pick the switch randomly so that output error behaves as white noise uncorrelated with the input digital word [3]. The same idea is used for the other input digital words, where the switches to be closed are selected randomly.

Our approach uses this technique but also take advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static view point. Since the output of the DAC is used as the input of the ADC, the same digital word using different randomly chosen current sources is going to be input to the ADC more than once. The ADC's output for each one of them is then stored for calculating the INL later. In this way the real-time limitations are eliminated and an arbitrarily accurate input signal can be generated.

The INL is calculated using the average value obtained for that particular transition point of the DAC that is input to the ADC. Since each individual value was generated using different combination of current sources, the average will be more accurate and will compensate part of the mismatching.

5. Simulations results

To verify our approach we simulated two flash ADCs with resistor mismatches. These ADCs are tested using simulated current mode thermometer-coded DAC with static error mismatch in the current sources. The mismatch in all cases has a Gaussian distribution with a standard deviation of 0.2 and a mean value of 1.

The results shown in Table 1 and Table 2 were calculated using two different sets of 100 different DACs. Each set is used to characterize one of the ADC. As is stated in the tables, 100 different 6-bit DACs were used to characterize a 3-bit ADC, while 10-bit DACs were used to characterize a 7-bit ADC. In both cases the DACs used to estimate the INL have high nonlinearities as we wanted.

Each DAC has different current sources, although all of them have mismatches. For each DAC the current sources are picked randomly following the DEM approach and each digital word is input to the ADC (with different current sources configurations) P times.

Also the INL is calculated and then compared to the actual INL of the ADC. This actual ADC INL is known since we know the ADC. For every DAC, an INL error is calculated using the difference between the actual ADC INL and the one estimated using our approach.

The average of the INL error for 100 different DACs and the worst error en the INL estimation are the values shown in Table 1 and Table 2.

Table 1: Results for a 3-bit ADC and 6-bit DACs.

3-bit ADC		
6-bit DAC		
Average DACs INL: 1.229023 LSB		
Worst DAC INL: 2.592191 LSB		
ADC actual INL: 0.832937 LSB		
P	Average error in ADC INL estimation [LSB]	Worst error in ADC INL estimation [LSB]
1	0.078160	0.292063
4	0.051692	0.183192
16	0.019900	0.081034
32	0.018850	0.074748

Table 2: Results for a 7-bit ADC and 10-bit DACs.

7-bit ADC		
10-bit DAC		
Average DACs INL: 5.812044 LSB		
Worst DAC INL: 12.846913 LSB		
ADC actual INL: 2.503805 LSB		
P	Average error in ADC INL estimation [LSB]	Worst error in ADC INL estimation [LSB]
1	0.147856	0.45451
32	0.08904	0.264553
128	0.083385	0.142052
512	0.083089	0.115538
1000	0.084044	0.107552

Same behavior is observed in the results shown in Table 2. INL estimate improves when the same DAC input digital word with different sources connected randomly is input to

the ADC. There is always an error present since the input is generated by a DAC and is not continuous.

From these results we can observe that minimal performance requirements are needed in the DEM DAC use to generate the input signal to the ADC. This make the approach practical for the use in a BIST environment since the area requirements for a no accurate ADC are not high.

6. Summary

In this paper we state and validate through simulations a technique to estimate the INL of an ADC using a DAC less accurate than the ADC. This technique uses DEM and also redundancy of samples, obtaining an arbitrary precision since DEM is not use in real-time single path. We believe that this technique can be used for testing ADCs with low quality DACs and can ease design of the testing circuits. Then the technique is well suited for BIST applications and production test environments.

7. References

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CHAPTER 3: A DETERMINISTIC DYNAMIC ELEMENT MATCHING APPROACH TO ADC TESTING

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Beatriz Olleta, Lance Juffer, Degang Chen and Randall Geiger

Abstract

A deterministic dynamic element matching (DEM) approach to ADC testing is introduced and compared with a common random DEM method. With both approaches, a highly non-ideal DAC is used to generate an excitation for a DUT that has linearity that far exceeds that of the test stimulus. Simulation results show that both methods can be used for testing of ADCs but with a substantial reduction in the number of samples required for the deterministic DEM method. This technique of using an imprecise excitation to test an accurate ADC offers potential for use in both production test and BIST environments.

1. Introduction

The conventional approach to testing analog-to-digital converters (ADCs) is a non-trivial task when following the conventional wisdom that a very accurate input is needed. This input is typically generated by a digital-to-analog converter (DAC) with substantially higher resolution than the device under test (DUT). Following this approach in a Built-In Self-Test (BIST) environment, the real challenge is in designing the circuit to test the part since it needs to have substantially higher resolution and linearity than the DUT. In a BIST application, the high performance requirement of DAC often translates into an expectation that the DAC needs more silicon area than the ADC to be tested.

It has been demonstrated that dynamic element matching (DEM) can be used to generate analog signals with high "average" SFDR using moderately low-linearity digital-to-analog converters [1]. This is because the randomizing effect of DEM spreads the errors in the DAC over a wide spectrum so that higher SFDR becomes possible. In [1], it was

specifically shown that, in a DAC with static errors, performance can be improved using random DEM. This characteristic of the dynamic element matching technique makes it a suitable candidate for generating the input of a DUT using a not-so-accurate DAC, and hence without the need of large silicon area and careful design of the test signal generator. A test strategy was recently introduced to use random DEM in a highly-nonlinear DAC to test high-resolution ADCs [2]. This work focuses on introducing the deterministic DEM testing technique and comparing it with the random DEM testing approach when a low accuracy DAC is used to characterize/test an ADC with higher linearity.

In the proposed schemes, the DAC will have nominally more bits of resolution than the ADC but it is not ideal due to large static errors caused by mismatch. Static mismatch errors can be caused by process variations and result in a nonlinear transfer curve in the DAC as characterized by the integral nonlinearity (INL). Although any number of ADC performance parameters may be characterized, in this work we will restrict the focus to INL performance with both proposed testing schemes.

This paper is organized as follows. An explanation of how the ADC is implemented and how the INL is calculated is given in Section 2. The dynamic element matching method is explained in Section 3. Details are presented in Section 3 about both the random and deterministic DEM implementations of the DAC, while in Section 5 simulation results are shown and discussed.

2. ADC model and INL calculation

To test both methods, a flash ADC is characterized through the INL measurement as in [2]. A simple implementation of a flash ADC is shown in Figure 1.

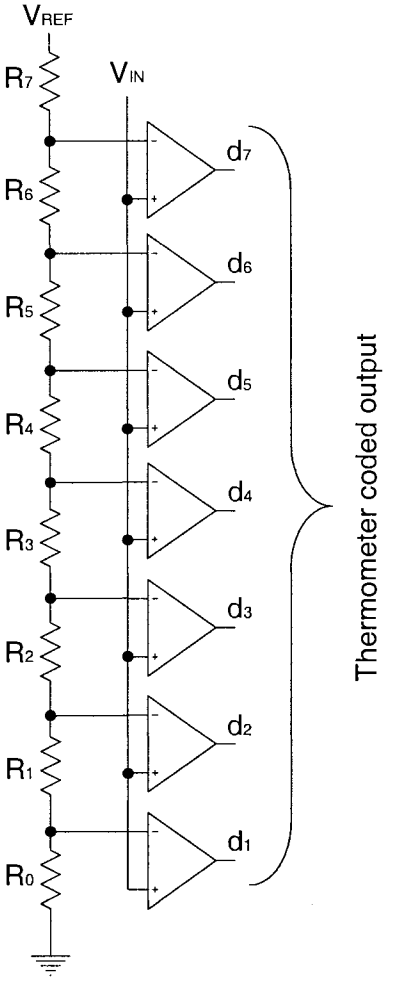

Figure 1: A 3-bit flash ADC.

The input signal to a flash converter is fed to the comparators in parallel. Each comparator is also connected to a resistor string, as shown in Figure 1. The output of the comparator is set to one if the input value is bigger than the voltage at the respective node of the resistor string, otherwise it is set to zero. The output code obtained is called a thermometer code. Resistor mismatches and comparator errors are the two primary sources of static errors in the ADC. However, since this paper focuses on INL and comparator errors do not accumulate into large INL, only the static error caused by resistor mismatches is modeled.

There are several alternative but similar definitions of the INL of an ADC. The endpoint fit line method is used for this work. In this definition, the INL, as given in (1), is

defined to be the maximum deviation of the ADC's transfer curve from the endpoint fit line, $V_{FITLINE}$. With this definition, the INL of an ideal ADC is 0.5 LSB.

$$INL = max\left(\left|\frac{V_o - V_{FITLINE}}{V_{LSB}}\right|\right) \quad (1)$$

An example of a non-ideal ADC transfer curve and its corresponding fit line are shown in Figure 2. It is a 3-bit flash ADC with a voltage reference equal to 2V.

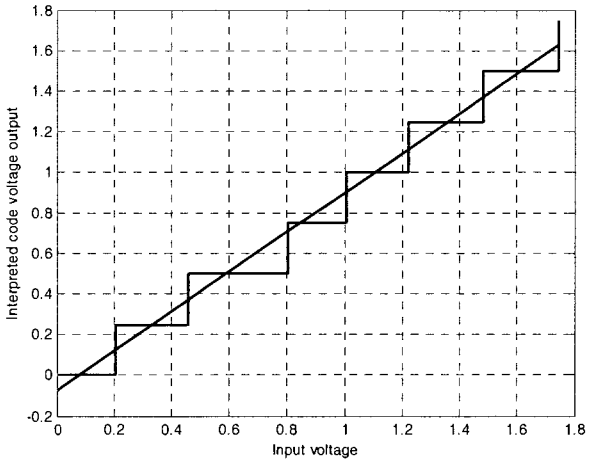

Figure 2: A non-ideal ADC transfer curve and its endpoint fit line.

As can be seen in Figure 2, the INL has local maximum values at the transition points when the output changes from one code to the next one. These are the points that need to be measured for characterizing the ADC under test.

3. Dynamic element matching

Element matching errors are inevitable due to inherent process variations. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The dynamic element matching technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average all element values are nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated in some applications.

Existing DEM structures are used in real-time circuits making it difficult to fully exploit DEM potential since in short time intervals the mismatch still substantially degrades performance. Our approach is different since the DEM is not in the DUT but in the signal generator used to test it, eliminating the real-time concern when using DEM.

4. A DAC with dynamic element matching

In order to construct a DAC with dynamic element matching, two different approaches can be found in the literature [1-3]. One is the partial randomization DEM. The other is the so-called full randomization DEM. This latter technique is one of the two techniques used in this work and will be explained next along with some modifications as seen in [2].

The full randomization DEM will be explained using a 3-bit current steering thermometer-coded DAC as an example as shown in Figure 3.

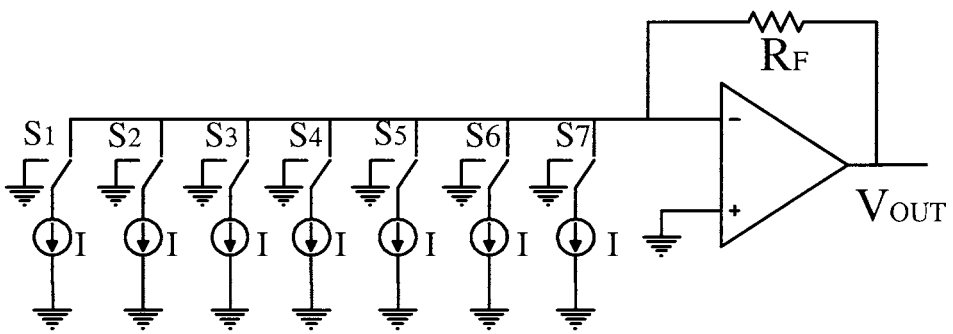

Figure 3: A 3-bit current mode thermometer-coded DAC.

In this case, when all switches are connected to ground, the output corresponds to the digital word zero. To generate the output voltage for the digital one, one switch needs to be connected to the inverting input of the operational amplifier (op amp). If the resistors and switches are matched, for a digital "k", any k of the switches needs to be connected to the inverting input. The resistor R_F is picked so that when all of the currents sources are on, the voltage output is at the desired maximum expected. The dynamic element matching idea for generating an output for a digital word "k" is to pick the switch location of k switches randomly each time an output corresponding to k is desired and then turn on these k

switches. In this way, the average output error for any k behaves as white noise uncorrelated with the input digital word [3]

Our approach uses this technique but also takes advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static viewpoint. Since the output of the DAC is used as the input of the ADC, the same digital word, using different randomly chosen current sources, is going to be input to the ADC more than once. The ADC's output for each one of them is then stored for calculating the INL later. In this way, the real-time limitations are eliminated, and an arbitrarily accurate average input signal can be generated.

The second method implemented for this work picks the current sources to be switched deterministically. The pattern used attempts to distribute the sources to be switched on in a way that all sources are used uniformly. In this case, as in the first approach, the same input code is used more than once and the output results are stored for INL calculation. The INL is calculated using the average value obtained for that particular transition point of the DAC that is input to the ADC. Since each individual value was generated using a different combination of current sources, the average may be more accurate and may compensate for part of the mismatch. It can be shown that this approach can also yield arbitrarily accurate input linearity for some deterministic selection sequences.

5. Simulations results

To verify our approach, we simulated flash ADCs with resistor mismatch. These ADCs were tested using a simulated current mode thermometer-coded DAC with static error mismatch in the current sources. The mismatch ratio for the ADC resistors and the DAC current sources both had a Gaussian distribution with a standard deviation of 0.2 and a mean value of 1. The simulated ADCs and DACs had 7 and 10 bits of resolution respectively.

5.1. No Calibration of DACs

As a baseline, the testing of one ADC from our sample of 100 was selected and tested with 100 DACs. The sample ADC had an INL of 2.9LSB. The results are shown in Fig. 4. As expected, the high level of nonlinearity in the DACs caused a large error in testing of the ADC with a worst case error of 1.293 LSB and an average error of 0.524 LSB.

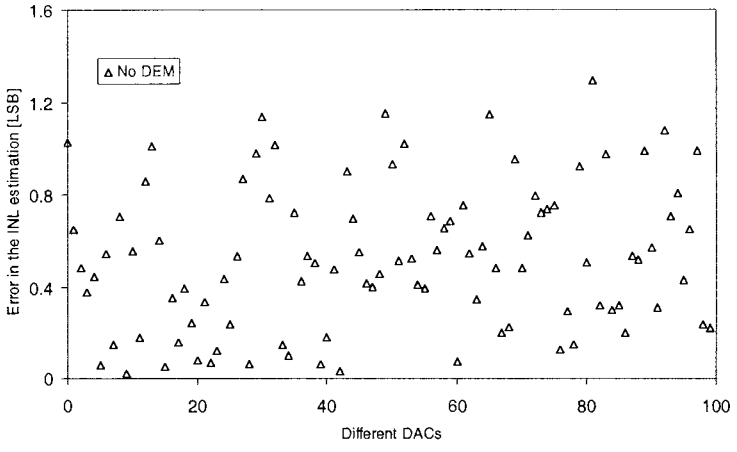

Figure 4: Error in the estimation of the INL of a given ADC for 100 different DACs without DEM.

5.2. Random DEM testing

In this test, one of the ADCs was selected and random DEM of the current sources in the DAC was used for testing the ADC. The test ADC had an INL of 2.9LSB. Each DAC has 1023 current sources. For each DAC the current sources were picked randomly following the DEM approach and each digital word was input to the ADC (with different random current source configurations) P times. The INL of the ADC was calculated and then compared to the actual INL of the ADC. In the simulation, the actual ADC INL was known since we know the transfer characteristics of the ADC. For every DAC, an INL error was calculated using the difference between the actual ADC INL and that estimated using the DEM approach. In Figure 5 the error in the calculation of the INL using 100 different 10-bit DACs is shown. In this set, the worst case INL of the DACs was 10.056 LSB at the 10-bit level. It can be seen that the random DEM algorithm estimated the INL of the 7-bit ADC to within 0.454 LSB in all 100 runs with P=8 random current source samples for each input code and to within 0.142 LSB with P=128 random current source samples.

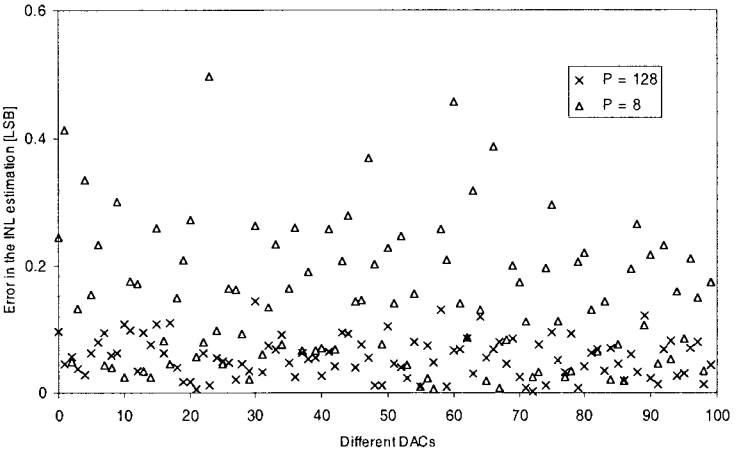

Figure 5: Error in the estimation of the INL of a given ADC for 100 different DACs using random DEM.

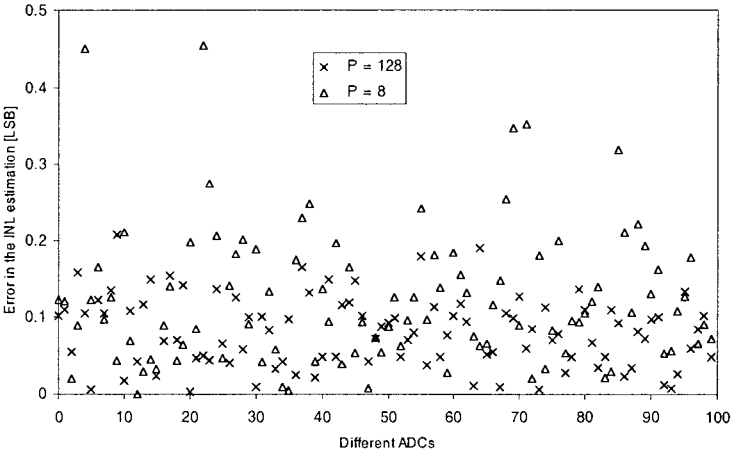

Figure 6: Error in the estimation of the INL of 100 different ADCs for a given DAC using random DEM.

In an attempt to assess the robustness of the algorithm, we then selected one DAC, the one with a worst-case INL of 10.056 LSB and used it to test the 100 ADCs that had INLs which ranged from 1.3 LSB to 4.3 LSB. The results are shown in Figure 6. As can be seen in both figures, when P equals 128, the error in both cases is less than 0.207 LSB, while for P equal to 8 the error is under 0.495 LSB. This can be contrasted to the P equals 1 case, i.e. no DEM, where the error was as high as 1.293 LSB in these 100 samples. It should be noted

that the DAC with an INL of 10.056 LSB at the 10-bit level corresponds to an INL at the 7-bit level of 1.3 LSB. Thus, an excitation that has a nonlinearity of 1.3 LSB can be used to measure the INL of an ADC at a substantially higher resolution level.

5.3. Deterministic DEM testing

In the deterministic DEM approach, the current sources are picked in a deterministic way to create the input words to the ADC. The deterministic selection was based solely on position of the current sources and not on the particular mismatch characteristics of a given DAC. Due to space limitations, details about how the current sources were spatially selected will not be given in this paper. Again each word was input P times, each with different configurations of the current sources. Results are shown in Figure 7 for the single ADC with a 2.9 bit INL and 100 DACs and in Figure 8 for the single DAC with 10.056 LSB INL and the 100 ADCs. The DACs and the ADCs were the same as used in the random DEM testing.

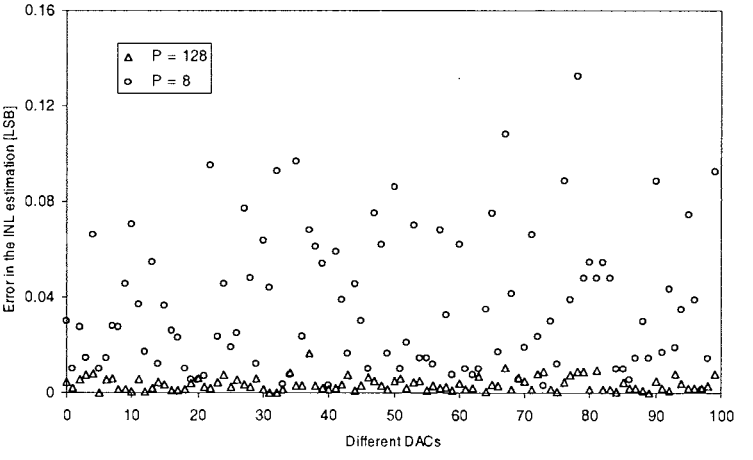

Figure 7: Error in the estimation of the INL of a given ADC for 100 different DACs using deterministic DEM.

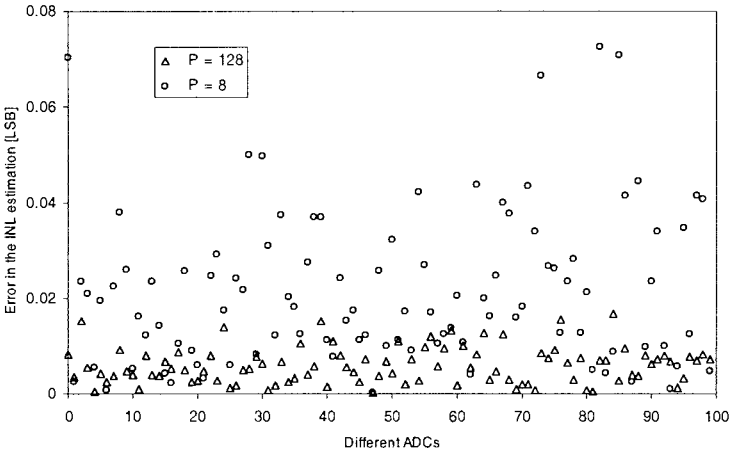

Figure 8: Error in the estimation of the INL of 100 different ADCs for a given DAC using deterministic DEM.

We see in these figures that the performance of this approach is significantly better than that obtained using randomly picked current sources in the DAC. The error is less than 0.017 LSB for all 100 DACs when P equals 128 and less than 0.132 LSB for P equals 8. Correspondingly, the error was 0.017 LSB when P equals 128 for the 100 ADCs and 0.072 LSB when P equals 8 for the same ADCs.

5.4. Comparison of random and deterministic DEM testing

A direct comparison of the random and deterministic DEM testing of the 100 ADCs was also made. In Figure 9 we compare the performance of estimating the INL for P=128 and in Fig. 10 for P=8. In these comparisons, the same DAC used in the previous sections with an INL of 10.056 LSB was used.

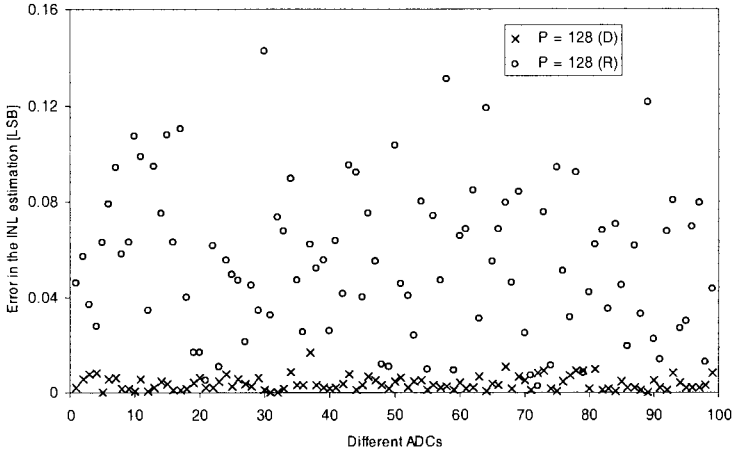

Figure 9: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 128.

From these figures, two important observations can be made. The deterministic DEM method offers substantial improvements in performance over that of the random DEM approach for a given number of samples. Second, it can be seen that the performance of the deterministic DEM approach with P equals 8 is comparable to that of the random DEM approach with P equals 128. This latter result is important, since substantially less testing time is needed which should be of particular benefit in a production test environment.

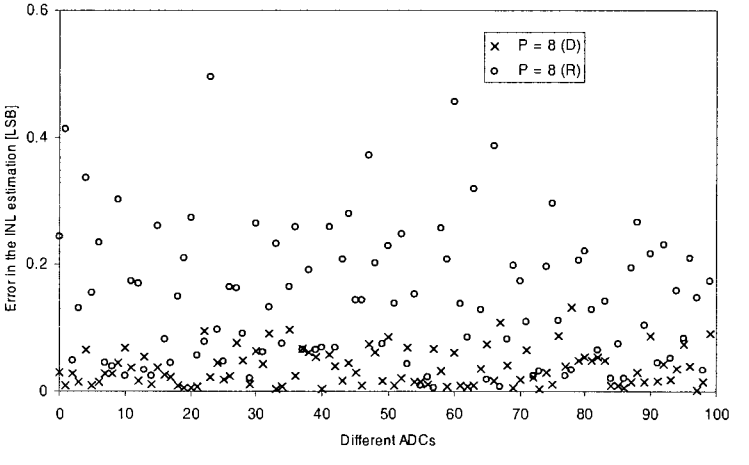

Figure 10: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 8.

Whether the specific spatial current source selection algorithm used for the deterministic DEM approach in these simulations is optimal or not has not been studied but even in its present form it offers substantial improvements over what is attainable with the random DEM approach.

6. Summary

In this paper we introduced a deterministic DEM method for testing ADCs and compared this technique with a recently introduced random DEM testing strategy. With this approach, DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADC. In both test strategies, the DEM is not used in real-time single path thus circumventing some of the limitations related to "specification averaging" inherent in using DEM for real-time signal processing. Through simulations, it was observed that the performance of the deterministic DEM method is substantially better from a testing viewpoint than what is attainable with a standard random DEM approach but both approaches offer major improvements over what can be achieved using the same DAC with no dynamic element matching involved. These techniques offer potential for use both in BIST and production test environments.

7. References

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CHAPTER 4: A DETERMINISTIC DYNAMIC ELEMENT MATCHING APPROACH FOR TESTING HIGH RESOLUTION ADCS WITH LOW ACCURACY EXCITATIONS

A paper to be submitted to IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing

Beatriz Olleta, Hanjun Jiang, Degang Chen and Randall L. Geiger

Abstract

Dynamic element matching (DEM) is an effective approach to achieving good average performance in the presence of major mismatch in matching-critical circuits but the approach has received minimal industrial adoption because of challenges associated with implementation of the randomizer and because of the time-local stationarity in signal path applications. This paper presents a DEM approach to ADC testing in which low precision DEM DACs are used to generate stimulus signals for the ADCs under test. Since the DEM is not in the signal path of the device under test (DUT), very high precision test results can be obtained. In addition to traditional random DEM techniques, a deterministic DEM (DDEM) strategy that offers substantial reductions in testing time is introduced. The performance of the DDEM method is mathematically formulated and the approach is validated with detailed simulation results that show the number of test vectors needed with this approach is comparable to what are currently used with standard code density linearity testing. It is demonstrated that both the random and deterministic DEM methods can be used to accurately test ADCs with linearity that far exceeds that of the DAC used as a signal generator. This technique of using an imprecise excitations and DEM to test much more accurate ADCs offers potential for use in both production test and BIST environments where high linearity devices are difficult to test and characterize.

1. Introduction

The International Technology Roadmap for Semiconductors [1] recognizes Analog-to-Digital Converters (ADCs) as the world's largest volume mixed-signal circuit. For example, ADCs are widely used in communications and signal processing circuits and systems. With the increasing complexity of mixed-signal circuits and the emergence of low-cost mixed-signal IC market, testing of analog and mixed-signal circuits in general and ADCs in particular has become a challenging and costly process [2]. Long test time and large investment on commercial mixed-signal testers have resulted in the need for alternate testing strategies.

Built-in-self-test (BIST) structures offer potential solutions not only in terms of reduction of costs associated with using testers, but also in terms of its ability to test deeply embedded systems on a chip (SOCs) and provide additional self-calibration facilities resulting in value addition of the parts [3]. There have been many attempts in providing BIST solutions for ADCs, most existing approaches in the literature have been aimed at duplicating a standard tester on chip [4] [5]. However, these methods have had little success and the 2001 ITRS states that design for test and BIST for analog and mixed-signal circuits are essentially unsolved [1].

In the conventional approach to testing ADCs, a highly accurate signal is required to stimulate the device under test (DUT). This stimulus input is typically generated by a digital-to-analog converter (DAC) with substantially higher precision than that of the DUT. In duplicating the production testing approach, most existing BIST approaches also require signal generators that have substantially higher resolution and linearity than the DUT. This becomes a significant challenge since such high performance signal generators require more design effort and more silicon area than the ADC to be tested.

Recently, we have developed a new philosophy for achieving analog and mixed-signal BIST. The basic idea of the new approach is to dramatically reduce the accuracy requirement on the signal generator and then use systems and signal processing techniques to accurately characterize and test the DUT. In [3], an algorithm was developed that takes advantage of redundancy in two nonlinear input signals to accurately test ADCs. In [6], the proposed algorithm explores the spatial frequency separation of the nonlinear input from the

DUT to characterize the ADC to accuracies that far exceeds the linearity of the stimulus. The mathematics behind linearity testing of ADCs using non-linear signals is presented in [7]; where a nonlinear stationary excitation and its shifted replica are needed. Simulations and experimental results validate the work as shown in [7]. In [8] a more rigorous analysis of the methods actually used and the new approach is done by the authors. In this paper we will present new dynamic element matching (DEM) techniques for using low accuracy DACs to achieve very high accuracy in ADC testing.

The DEM method was used by H. T. Jensen and I. Galton [9] [10] to improve the effective specifications of linearity performance of DACs. For example, it has been demonstrated that DEM can be used to appreciably improve the SFDR performance of moderately low-linearity DACs [9]. This is because the randomizing effect of DEM spreads the errors in the DAC over a wide spectrum so that higher SFDR becomes possible. Other researchers use DEM on Delta-Sigma Converters. Adams and his colleagues applied DEM on oversampling DAC where he uses noise shaped scramblers to achieve high SNR [11]. Z. Li and T. S. Fiez have studied different DEM algorithms in [12], while a new algorithm is introduced and analyzed on [13] by R. T. Baird and T. S. Fiez. A $\Sigma\Delta$ DAC is implemented using a new algorithm in the work by R. E. Radke, A. Eshraghi and T. S. Fiez in [14].

Although there have been concerns about using DEM to create "effectively linear" devices since the actual nonlinearity in the signal path is not removed, we believe the "averaged linearity" provided by DEM can be exploited to generate "effectively linear" stimulus signals for ADC testing. This approach allows the signal generator to be realized with a not-so-accurate DAC, hence eliminating the need of large silicon area and careful design of the test signal generator. In a preliminary study, a test strategy was introduced to use random DEM in a highly-nonlinear DAC to test low-resolution ADCs [15]. A new deterministic DEM testing technique was also introduced and compared with the random DEM testing approach when a low accuracy DAC is used to characterize/test an ADC with higher linearity in [16]. In this work the deterministic and random DEM algorithms are explained in detail with mathematical proof of its behavior. Also simulations for high resolution ADC characterization using deterministic DEM are shown in this work.

In the proposed scheme, the DAC will have nominally more bits of resolution than the ADC but it is not ideal due to large static errors caused by mismatches. Static mismatch errors can be caused by process variations and result in a nonlinear transfer curve in the DAC as characterized by the integral nonlinearity (INL). Although any number of ADC performance parameters may be characterized, in this work we will restrict the focus to INL performance.

This paper is organized as follows. An explanation of how the ADC is implemented and how the INL is calculated is given in Section 2. The dynamic element matching method is explained in Section 3. Details are presented in Section 4 about both the random and deterministic DEM implementations, along with mathematical derivation, algorithm description and simulation results. In Section 5 simulation results for a high resolution ADC are shown and discussed using only the deterministic DEM testing. Section 6 summarizes present and future work in this area.

2. ADC Model and INL calculation

Although the proposed DEM methods for generating stimulus signals can be used to test any types of ADCs, this paper will focus on flash ADC testing. The reason behind this choice is the belief that the linearity testing of a flash ADC is more challenging because of the random nature of its nonlinearities. Once developed for flash ADCs, the method can be easily extended to pipelined ADCs and successive approximation structures, since it relies only on the transition points of the real ADC.

Consider a simple 3-bit flash ADC shown in Figure 1. The input signal to a flash converter is fed to the comparators in parallel. Each comparator is also connected to a tap voltage on a resistor string, as shown in Figure 1. The output of the comparator is set to one if the input voltage is higher than the tap voltage, otherwise it is set to zero. The output code thus obtained is called a thermometer code which is then converted to a binary number between 0 and 7. When the ADC input V_{IN} is gradually increased from 0 to V_{REF}, the ADC output code X_o follows a staircase curve called the DC transfer curve of the ADC, as shown in Figure 2 for $V_{REF} = 2V$. Here we assume that the ADC is monotone.

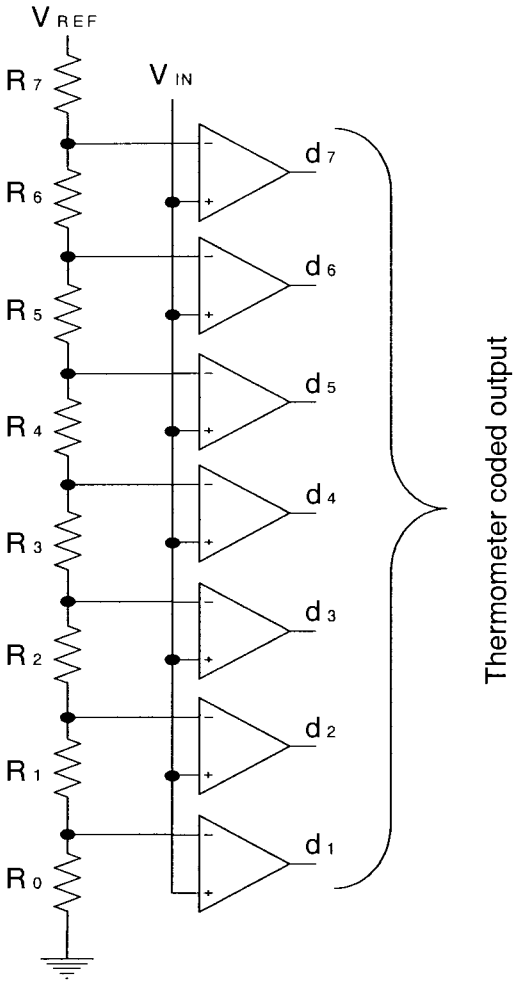


Figure 1: A 3-bit flash ADC.

The transition voltages on the DC transfer curve correspond to the tap voltages on the resistor string, if the comparator offsets are neglected (since they do not accumulate and can be modeled as additive noise at the ADC input). Ideally, each resistor has exactly the same resistance, resulting in transition voltages that are evenly separated on the horizontal axis. Resistor mismatches cause the actual transition voltages to differ from their ideal levels. Such errors are referred to as the integral non-linearity (INL) errors of the ADC.

There are several alternative but similar definitions of the INL of an ADC. In some cases [17], the INL is defined as a continuous time function of the ADC input voltage, whereas in other cases, the INL is only defined at the ADC's transition points thus resulting in a discrete-time function INL_k. In this paper, we follow what is most commonly used by

industry test engineers and use the transition point INL_k to characterize the ADC's linearity performance. For completeness, the INL_k definition is given as follows.

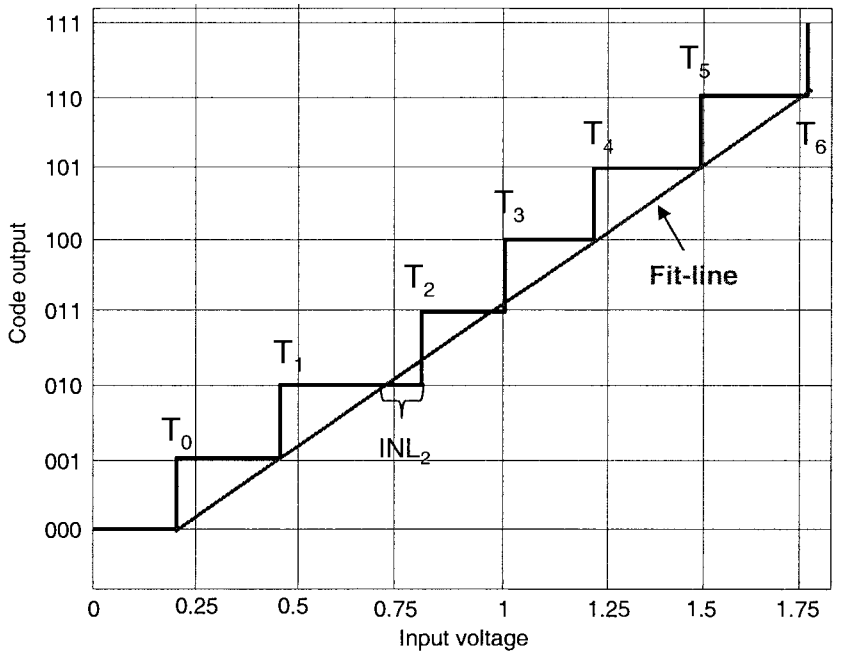


Figure 2: A non-ideal ADC transfer curve and its fit line.

To define the INL_k of the ADC, we first need the transition points of an ideal linear ADC which are usually defined as the endpoint-fit line transition points I_k:

$$I_k = T_0 + \frac{T_{N-2} - T_0}{N-2} k, \qquad k = 0,1...N-2 \qquad (1)$$

Equation 1 represents a straight line connecting the first and last transition points of the ADC, as seen in Figure 2. Actual transition points of an ADC are compared to their corresponding endpoint-fit line transition points for linearity characterization. The difference between the actual transition points and the fit-line transition points is defined as INL_k and is expressed in LSBs. This definition automatically eliminates the dependence on exact values of the first and last transition points. INL_k is defined mathematically by:

$$INL_k = \frac{T_k - I_k}{1\,LSB} = \frac{T_k - T_0}{T_{N-2} - T_0}(N-2) - k \qquad (2)$$
$$k = 1,2...N-3$$

Notice that by definition the INL_k for the first (k=0) and last (k=N-2) transition points are 0 and they do not appear in equation 2.

The most commonly used method for ADC INL testing is the standard histogram method and that is also the method that we will use in this paper to test ADC linearity. In the standard use of the histogram method, an ideal linear ramp signal is presented to the input of the ADC. The ADC takes samples of the input and the converted output codes are tallied into corresponding bins. Since V_{in} is proportional to time and the sampling intervals are constant, the total number of accumulated samples is proportional to V_{in}. Therefore a transition voltage is proportional to the total code hits for all output codes corresponding to lower voltages, and the accumulated histogram counts can be directly used to compute the INL_k of the ADC.

Naturally, in order for this method to work, it is imperative to have a highly linear ramp, with linearity a decade or more better than that of the ADC under test, since any nonlinearity in the input signal will be directly translated into INLk estimation error in the histogram method. If the ramp is generated using a DAC, it is required that the DAC have resolution and linearity that are at least 3 bits more than the targeted resolution of the DUT. This is a fundamental challenge in both production test and built-in-self-test of high resolution ADCs.

This paper presents methods to overcome this challenge by allowing the use of low linearity DACs for high accuracy testing of ADCs. Furthermore, our method will allow exactly the same signal processing algorithm as used in the histogram method to be used in estimating the ADC's linearity performance. This is possible because the proposed deterministic DEM method will enable a nonlinear DAC signal source to generate a nearly identical histogram at the ADC output to what an ideal linear ramp would.

3. Dynamic element matching

Element matching errors are inevitable due to inherent process variations. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The dynamic element matching technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average all element values are

nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated in some applications.

Consider for example the situation where a capacitance ratio $r = \frac{C_1}{C_2}$ of 1 is needed. However, due to inevitable variations, we have $C_1 = C_0(1+\Delta_1)$, $C_2 = C_0(1+\Delta_2)$, and Δ_1 and Δ_2 are random variables with mean equal to 0 and variance inversely proportional to the area used. One way to improve the accuracy of r is to increase the area of the capacitors. The dynamic element matching method takes a totally new approach. In the DEM approach, the area for the capacitors is divided into several, say 8, smaller areas so that 8 instead of 2 smaller capacitors are built with the same amount of area. During the real time operation, switches are dynamically turned on and off so that 2 out of the 8 capacitors are selected to create the capacitance ratio $r(t) = \frac{C_{i(t)}}{C_{j(t)}}$ in each clock period. The selection of the 2 capacitors is typically randomized. If the random selection is done so that the probability of selecting any 2 capacitors is the same, we have the averaged value or the expected value of the capacitor ratio as given by

$$\bar{r} = \frac{1}{56}\left(\frac{C_1}{C_2} + \frac{C_2}{C_1} + \frac{C_1}{C_3} + \frac{C_3}{C_1} + \ldots + \frac{C_7}{C_8} + \frac{C_8}{C_7}\right)$$

$\bar{r}$ will be much closer to 1 than the original r since whenever there is a ratio greater than 1 $\left(say\ \frac{C_1}{C_2}\right)$ there is also a ratio less than 1, $\left(\frac{C_2}{C_1}\right)$ to be averaged together. Furthermore, this significant improvement in the ratio accuracy is achieved without using extra area. In fact, the individual capacitors switched in are smaller than their original sizes, potentially leading to faster operation.

The basic idea of DEM has been used by various researchers in different applications. As an example we will mention the DEM concept as was explained in [9]. It is known that nonlinear circuit behavior introduces harmonic distortion, for example in a DAC output. In order to overcome this problem DEM can be applied to the DAC. The DAC proposed in [9] consists of 2^n 1-bit DACs, where n is the DAC resolution, and an analog output adder. The

1-bit DACs are used randomly using a digital control consisting of a thermometer code generator followed by a scrambler. The scrambler will change the ones that the thermometer coder inputs to it, so that in each clock period a different configuration of DACs is used. This randomly modulates the DAC noise, converting harmonic distortion into white noise. Fiez improves Sigma-Delta converters linearity using different DEM algorithms, in [13] the algorithm has no scrambler and the DAC elements are chosen sequentially beginning from the next available not-used element. This method can suffer from signal-dependent harmonic distortion. They overcame this problem in [14].

As was stated, existing DEM structures are used in real-time circuits making it difficult to fully exploit DEM potential since in short time intervals the mismatch still substantially degrades performance. Our approach is different since the DEM is not in the DUT but in the signal generator used to test the DUT, eliminating the real-time concern when using DEM.

4. Dynamic element matching testing

In order to construct a DAC with dynamic element matching, different approaches can be found in the literature [9-14]. Two methods were simulated and compared in [16], the so called random and deterministic dynamic element matching for testing.

To verify our approaches, we simulated flash ADCs with resistor mismatches. These ADCs were tested using a simulated current steering thermometer-coded DAC with static mismatch errors in the current sources.

In this section, we will first briefly describe the random DEM testing method. Then the deterministic DEM approach is described and its performance evaluated. The comparison of the two DEM approaches is also presented.

4.1 Random DEM Testing

The random DEM will be explained using a 3-bit current steering thermometer-coded DAC as an example as shown in Figure 3.

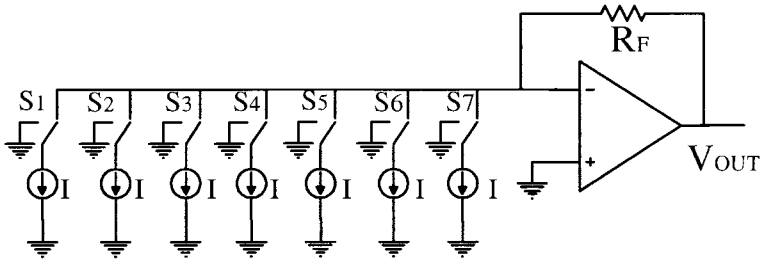


Figure 3: A 3-bit current mode thermometer-coded DAC.

In this case, when all switches are connected to ground, the output corresponds to the input digital word zero. The resistor R_F is picked so that when all of the current sources are on, the voltage output is at the desired maximum. To generate the output voltage for input digital word one, one switch needs to be connected to the inverting input of the operational amplifier (op amp). If the resistors and switches are matched, for a digital "k", any k of the switches needs to be connected to the inverting input. The random dynamic element matching idea for generating an output for a digital word "k" is to pick k switches randomly to be turned on each time an output corresponding to k is desired. We can have multiple outputs for each digital word 'k' with different randomly selected current sources. In this way, the output voltage error for any k behaves like noise uncorrelated with the input digital word [16]. The distribution of the noise depends on the characteristics of the matching errors and the switching sequence.

It should be pointed out that for this method both a thermometer coder and a randomizer (scrambler) are needed in order to implement the random switching of the sources.

Our DEM testing approach uses this technique but also takes advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static viewpoint, where the output of a DAC is used as the input of the ADC. We will define P as the number of times that the DAC's output for the same input digital word will be input to the ADC. Different randomly chosen current sources are switched each of the P times that the same code is input to the DAC. The ADC's outputs corresponding to each one of the P input samples are then stored for calculating the INL later. In this way, the real-time limitations are eliminated, and an accurate average input signal can be generated.

4.2 Deterministic DEM method for thermometer coded DACs

This section explains the deterministic DEM method that can be applied to thermometer coded DACs to improve the performance of the inaccurate DACs in the sense of averaging. Performance evaluation for the thermometer coded DACs with deterministic DEM is also given.

4.2.1 Description of deterministic DEM method for thermometer coded DAC

As pointed out earlier, a current steering DAC can be thermometer coded, binary coded or their combination. To get started, the deterministic DEM method was applied to a thermometer coded DAC. Suppose the DAC has n-bit resolution, then it has 2^n-1 current source elements. The DAC structure was already shown in Figure 3.

The deterministic method deterministically picks the current sources to be switched on. The pattern used attempts to distribute the sources to be switched on in a way that all sources are used almost uniformly.

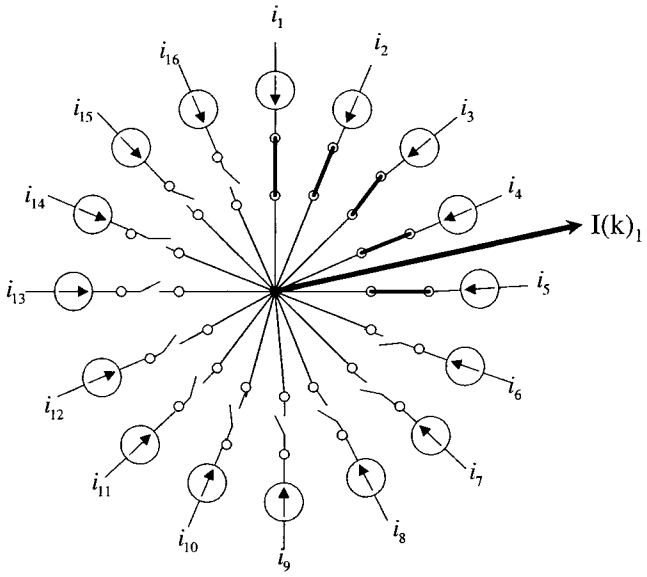
To perform the DDEM method, we add one more current source element to the DAC, and the DAC has totally 2^n current sources. Let $N = 2^n$. We use $i_j \quad (j = 1,..., N)$ to represent the j^{th} current source element out of the total N elements. As explained before, P represents the number of samples to be generated for each DAC input word. We define $q = N / P$.

The following deterministic DEM switching scheme was applied to the DAC current sources:

1. All current sources are arranged conceptually along a circle to visualize the wrapping effect (physical layout of the current sources can be a rectangular array). P starting places that are $q = N / P$ current sources are selected.
2. For each input code k, the DAC generates P samples of output. Each sample is obtained by switching k current sources consecutively starting from one of the P starting places. The d^{th} $(1 \le d \le P)$ sample is obtained by switching k current sources starting from $i_{(d-1)q+1}$ in the clock-wise direction.
3. The output analog signal is obtained by forcing the summation of the selected k current sources to drive a resistor R_F. Since the resistor value can be viewed as a

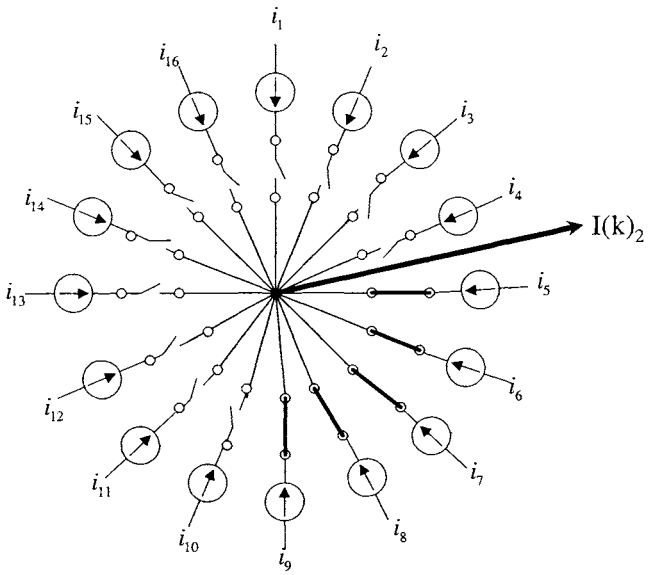
normalization factor, we only need to examine the current through it to evaluate the DAC performance.

Figure 4 illustrates the DDEM switching of a 4-bit DAC when the input code is 5 as an example. In this example, n = 4, N = 16, P = 4 and q = 4. Note that the current flowing direction is reversed from that shown in Figure 3. However, it will not affect the evaluation of the DDEM DAC performance since there is only a sign difference.

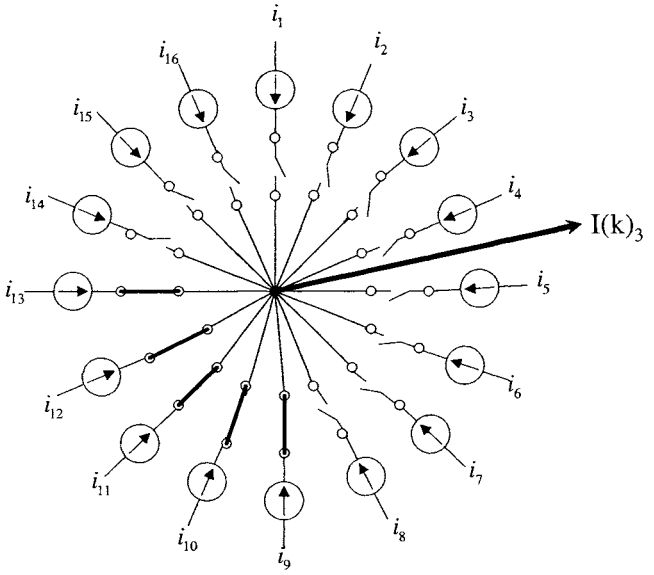


a) 1st output sample when k=5

Figure 4: Deterministic DEM switching of a 4-bit DAC

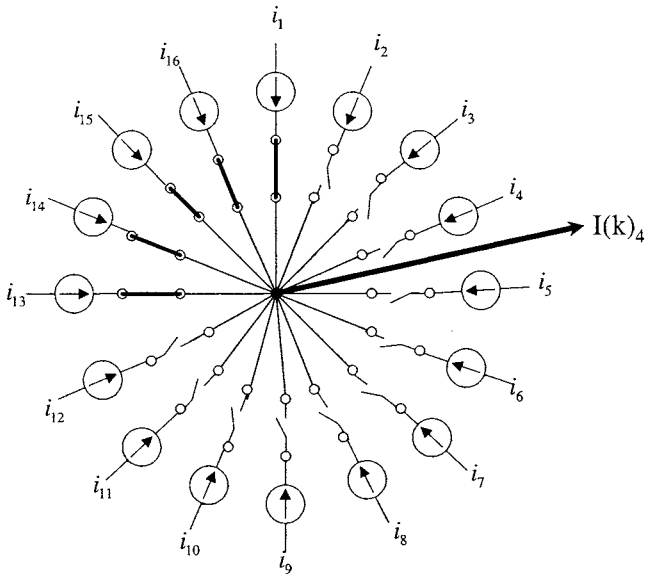


b) 2nd output sample when k=5



c) 3rd output sample when k=5

Figure 4: Deterministic DEM switching of a 4-bit DAC (continued)



d) 4th output sample when k=5

Figure 4: Deterministic DEM switching of a 4-bit DAC (continued)

The logic needed to implement this approach is much simpler than the one needed for the random case. No scrambler is needed and the on values are only shifted by a fixed amount, so a shift register could be used to store the on signals to the current sources. However, we must point out that when a high resolution DAC is needed, the number of switches, the size of the shift register and the routing increase exponentially. Then the DAC design starts to present new challenges and its area increases. Strategies addressing these and related issues are being studied. For now, let us focus on the DDEM concept and its performance potential.

As in the first approach, the same input code is used more than once and the output results are stored for INL calculation. The ADC's INL is calculated using the overall histogram data after all DAC input codes have been used. Since each individual DAC output value was generated using a different combination of current sources, the P samples are dispersed over a voltage range. Hence the P samples can be described by their average value plus a variation due to current source mismatches. We will show that this "average output"

has excellent linearity performance and the variations from the average can effectively increase the DAC resolution.

The static performance of the DAC will be evaluated based on $I_d(k)$ and $\bar{I}(k)$, which are defined next.

For each input code k, the DAC outputs P samples. Each output is nothing but the summation of the selected k current elements. The d^{th} current summation is denoted by $I_d(k)$. We have then that

$$I_d(k) = \sum_{j=1}^{k} i_{(d-1)q+j} \qquad d = 1,...,P \qquad (3)$$

The average of the P samples for a given code k is denoted by $\bar{I}(k)$

$$\bar{I}(k) = \frac{1}{P} \sum_{d=1}^{P} \sum_{j=1}^{k} i_{(d-1)q+j} \qquad (4)$$

4.2.2 Performance evaluation of the DDEM switched thermometer coded DAC

This subsection will formally show that the "averaged DAC" with our DDEM approach can generate a signal that is very close to being an ideal ramp, which means that the DC transfer curve of our "averaged DAC" is very close to a straight line. This is done by showing that the INL of the averaged DAC is very small. Remember that INL captures the deviation of the transfer curve from the straight fit-line. It must be stressed here that what we are going to proof is much stronger than saying the expected value of the averaged DAC output is on the fit-line, which is guaranteed by construction.

Before we start, let's suppose that the designed value, which is also the expected value, of all current sources is i_0. Due to process and other variations, the actual value of each current source is actually given by:

$$i_j = i_0(1+\varepsilon_j) \quad (j = 1,...,N). \qquad (5)$$

where each ε_j $(j = 1,...,N)$ is independent and has an identical Gaussian distribution. That is, we assume ε_j $i.i.d.$ $\sim N(0,\sigma^2)$ where σ^2 is determined by design and process variations.

We need to define the fit line for INL evaluation. The fit line of a DAC is the straight line connecting the DAC output voltages corresponding to the first and last DAC input codes. The first DAC input is 0, and the last DAC input code is N since we have totally N current source elements in the DAC. The DAC LSB is defined to be the voltage difference between these two codes divided by the number of transitions, N. Since the DAC output voltage is the output current times the output impedance, we can use the output current instead of voltage in all of our computations, if we assume that the output impedance is constant. The corresponding output for the input code 0 for our DAC structure is also 0. The output current with input code N for which all the N current sources are switched is given in equation (6):

$$I(N) = \sum_{j=1}^{N} i_j = N i_0 + i_0 \sum_{j=1}^{N} \varepsilon_j \qquad (6)$$

Therefore the LSB of the DDEM DAC is given by:

$$\overline{LSB} = \frac{I(N) - I(0)}{N} = i_0 + i_0 \frac{1}{N} \sum_{j=1}^{N} \varepsilon_j \qquad (7)$$

It can be verified that $\frac{1}{N} \sum_{j=1}^{N} \varepsilon_j$ is Gaussian and has the following standard deviation

$$\frac{1}{N} \sum_{j=1}^{N} \varepsilon_j \sim N(0, \frac{1}{N} \sigma^2) \qquad (8)$$

Since N is a very large number, the variation of $\overline{LSB}$ from i_0 is very small.

The fit-line of the DDEM DAC for each input code k is then given by:

$$\bar{I}_{fit}(k) = k \cdot \overline{LSB} = k i_0 + i_0 \frac{k}{N} \sum_{j=1}^{N} \varepsilon_j \qquad (9)$$

Once we have the fit line, we can now compute the INL of the DDEM DAC. This is done by calculating, for each DAC input code, the distance from the averaged value of the DACs output current to the corresponding fit line point. Let's denote this distance at code k by $\overline{INL(k)}$. When $k = tq + s$, $s = 1, \ldots, q$, $t = 0, \ldots, P-1$, the averaged DAC output current derived from equation (4) and (5) is given by

$$\bar{I}(k)=k\cdot i_0+i_0\cdot\frac{1}{P}\cdot\left(t\cdot\sum_{d=1}^{P}\sum_{j=s+1}^{q}\varepsilon_{(d-1)q+j}+(t+1)\cdot\sum_{d=1}^{P}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right)=$$

$$=k\cdot i_0+i_0\cdot\frac{1}{P}\cdot\left(t\cdot\sum_{j=1}^{N}\varepsilon_j+\cdot\sum_{d=1}^{P}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right) \quad (10)$$

Subtracting it by the corresponding fit line point yields

$$\overline{INL}(k)=\bar{I}(k)-\bar{I}_{fit}(k)$$

$$=i_0\frac{1}{P}\cdot\left(t\cdot\sum_{j=1}^{N}\varepsilon_j+\cdot\sum_{d=1}^{P}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right)-i_0\frac{k}{N}\sum_{j=1}^{N}\varepsilon_j$$

$$=i_0\left[\left(\frac{1}{P}-\frac{s}{N}\right)\sum_{d=1}^{P}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}-\frac{s}{N}\sum_{d=1}^{P}\sum_{j=s+1}^{q}\varepsilon_{(d-1)q+j}\right] \quad (11)$$

It can be proved that the distribution of the normalized $\overline{INL}(k)$ is given by:

$$\frac{\overline{INL}(k)}{i_0}\sim N\left(0,A\sigma^2\right)\quad where\qquad A=\left(\frac{1}{P}-\frac{s}{N}\right)^2Ps+\left(\frac{s}{N}\right)^2P(q-s)=\frac{s(q-s)}{Pq} \quad (12)$$

This formula shows that whenever s= q, that is, k is a multiple of q, the variance of $\overline{INL}(k)$ is equal to zero, meaning that the DDEM DAC output is exactly on the fit line. This is correct since when k=(t+1)q, t=0,…,P-1, each and every current source in the DAC will be used exactly t times among the P samples. Hence their averaged value will be exactly $k i_0$, with no uncertainty.

From equation (12), we can also estimate where and how much we expected the maximum deviation from the fit line to be. The variance of $\overline{INL}(k)$ reaches its maximum value at s = ½q. Using this value for s and with i_0 equals to 1 LSB, the largest standard deviation of $\overline{INL}(k)$ is $\sqrt{\frac{q}{4P}}\sigma=\sqrt{\frac{N}{4P^2}}\sigma$ (13)

It is known [18] that the distribution of the $\overline{INL}(k)$ for a non-DEM current steering DAC is given by

$$\frac{INL(k)}{i_0}\sim N(0,\frac{(N-k)k}{N}\sigma^2) \quad (14)$$

The largest standard deviation of $INL(k)$ is approximately $\frac{\sqrt{N}}{2}\sigma$.

When n=18, P=2^7=128 and q=2^{11}, we have $\sqrt{\frac{q}{4P}} = 2$ and $\frac{\sqrt{N}}{2} = 2^8$.

We can see how $\frac{\sqrt{N}}{2}\sigma$ is much larger than $\sqrt{\frac{q}{4P}}\sigma$.

The conclusion is that the $\overline{INL}$ of a DDEM switching DAC is greatly improved as compared with the INL of a non-DEM DAC with the same current source elements. Furthermore, the current sources can be built without using large area to ensure that their standard deviation is with 0.1 LSB. With such a DAC (which would have about 11 or 12 bit original linearity), the DDEM DAC will have 18 bit linearity with P=128. This proves that the proposed DDEM DAC can be used to generate a ramp, by increasing the DAC input code sequentially from 0 to N-1, with 18 bit effective linearity. The variation of the DAC output current among the P sample for the same code can be treated as an additive noise to the ideal ramp at the input of the ADC.

4.3 Comparison of random and deterministic DEM testing.

For the simulation the mismatch ratio for the ADC resistors and the DAC current sources both had a Gaussian distribution with a standard deviation of 0.2 and a mean value of 1. The simulated ADCs and DACs had 7 and 10 bits of resolution respectively. We limited ourselves to this low resolution because the random DEM becomes prohibitively too slower for higher resolution. A direct comparison of the random and deterministic DEM testing of the 100 ADCs was made. In Figure 7 we compare the performance of estimating the INL for P=128 and in Figure 8 for P=8. In these comparisons, a DAC with an INL of 10.056 LSB was used. The DAC used is a current steering thermometer-coded DAC.

From Figures 6 and 7, two important observations can be made. The deterministic DEM method offers substantial improvements in performance over that of the random DEM approach for a given number of samples using both DAC architectures. Second, it can be seen that the performance of the deterministic DEM approach with P equals 8 is comparable to that of the random DEM approach with P equals 128. This latter result is important, since

substantially less testing time is needed which should be of particular benefit in a production test environment.

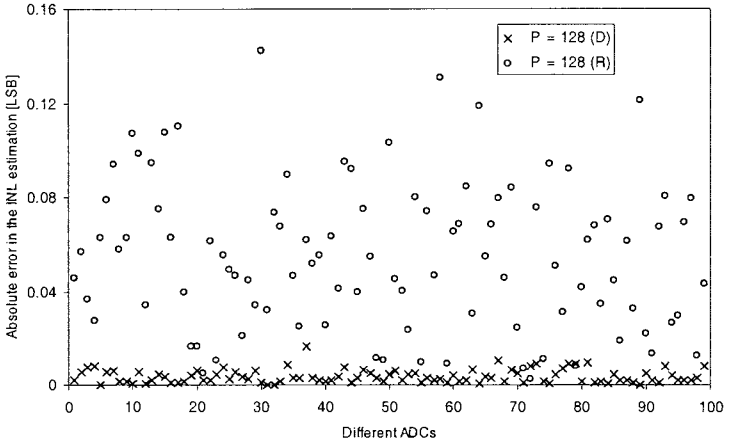


Figure 6: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 128.

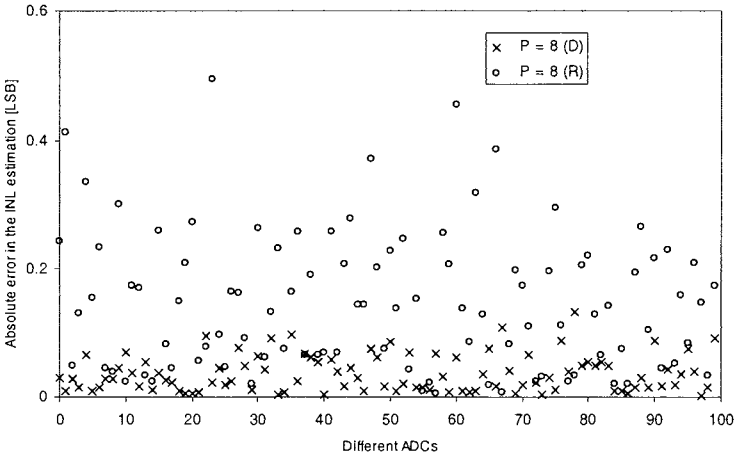


Figure 7: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 8.

Whether the specific spatial current source selection algorithm used for the deterministic DEM (DDEM) approach in these simulations is optimal or not has not been

studied but even in its present form it offers substantial improvements over what is attainable with the random DEM approach.

5. Deterministic DEM testing simulation results

Extensive simulations were run using only the DDEM testing scheme, since as was stated in last section it behaves better than the random DEM testing method and also take dramatically less computational effort and so simulations can be run for much higher resolution ADCs and DACs.

For the following simulation results, the ADCs have 16 bit resolution while the DACs have 18 bits of resolution (not accuracy!). All devices were simulated with mismatched errors in the ADC's resistances and in the DAC's current sources. The DAC output range is 1% bigger than the ADC input voltage range and noise was added to the DAC output.

First we generated one particular DAC and used it as the ramp signal generator to test 1000 randomly generated ADCs. The DAC current source mismatches have a Gaussian distribution with a standard deviation equal to 0.2 and a mean equal to 1. Each randomly generated ADC has a resistor string with individual resistances following a Gaussian distribution with standard deviation of 0.03 and mean value of 1. This gives us 16 bit ADCs with an average INL of 7.15 LSB with individual ADC's INL ranging from 3 and 16.1 LSB. The DAC used for the testing has an INL equal to 78 LSB. Figure 8 shows the histogram of the INL estimation errors for the 1000 different ADCs when the DAC used for testing has no DEM. Figure 9 and Figure 10 show how the errors in the INL estimation has been dramatically reduced when the same DAC was used for testing with the DDEM approach with P=32 and P=128 respectively.

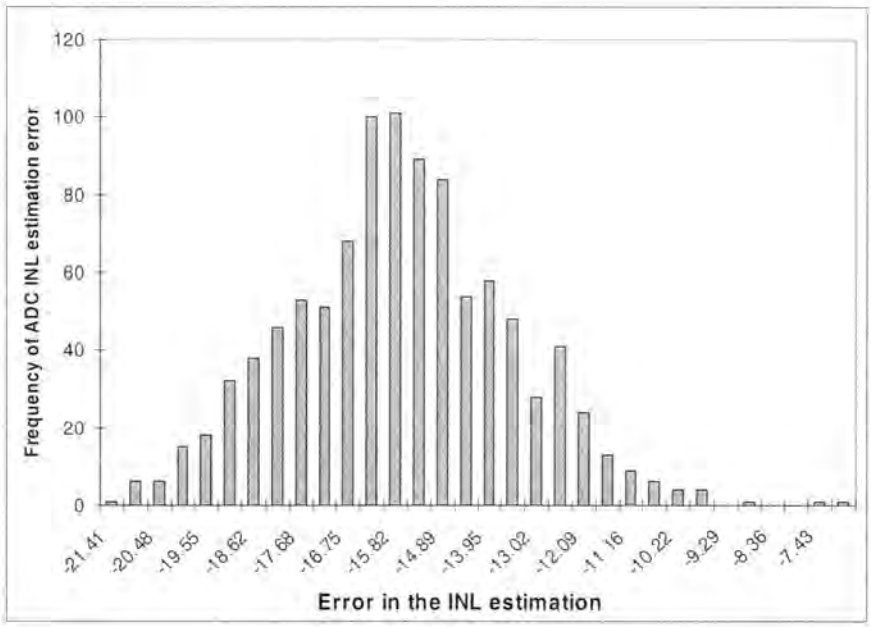


Figure 8: INL estimation error distribution when testing 1000 different ADCs using a NO DEM DAC.

As can be seen the errors in the estimated INL decreased by two orders of magnitude, from up to −21.4 LSB error to up to −0.88 LSB error for P = 32, and up to −0.23 LSB error for P = 128, when DDEM is applied in the DAC. We can see from the distribution that most the errors are actually between ±0.18 LSB for P = 128. Note also that in this case the linearity of the DAC is only 11 bits. Therefore, the proposed DDEM testing methods correctly tested the linearity performance of 1000 ADCs to accuracies at the 17 to 19 bit level, by using a DAC with only 11 bit linearity as a ramp generator. It is also worth pointing out that the algorithm used for computing the INL performance is the same as what is used in the standard histogram method for ADC INL testing, while the number of samples per code used in the testing is quite reasonable. Also we can see how increasing P helps to improve the obtained results as we expected; this could be useful since we can maintain good linearity with lower resolution DACs using bigger amount of samples. We want to keep the DAC resolution as low as possible so that it uses less area and also the switching implementation is less complex.

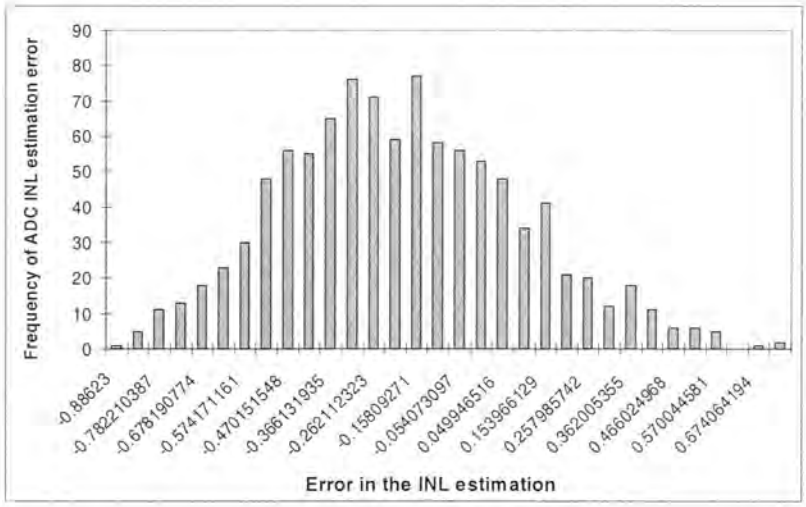


Figure 9: INL estimation error distribution when testing 1000 different ADCs using a DDEM DAC with P=32.

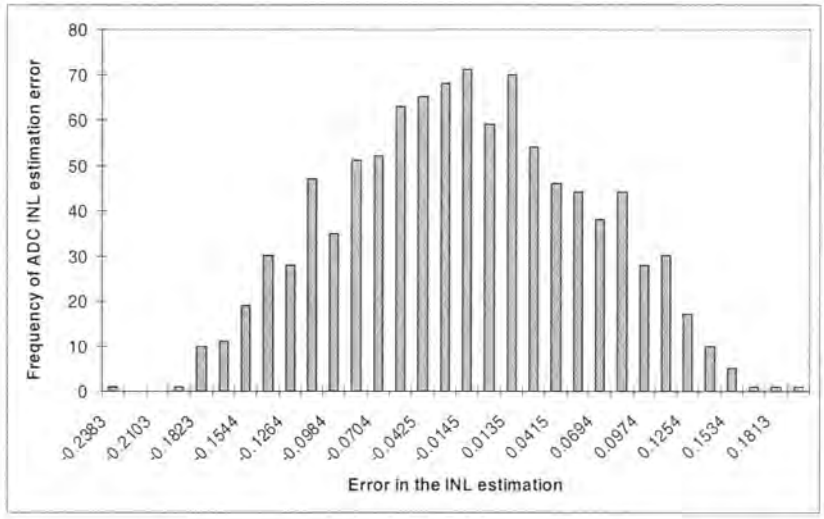


Figure 10: INL estimation error distribution when testing 1000 different ADCs using a DDEM DAC with P=128

To further show the accuracy of this method, the true and the estimated INL_k for one particular ADC is shown in Figure 11. We can see how the INL_k estimated follows the true INL_k for all k.

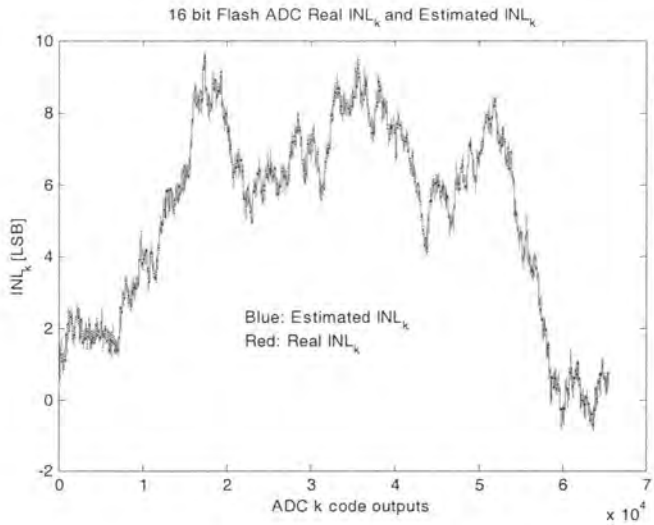


Figure 11: Estimated and real INL_k for a given ADC using a DDEM DAC with P=128

To verify the performance of the proposed technique as a test tool we simulated 1000 ADCs with INL around 0.5 LSB. The DAC use to estimate the ADCs' INL has an INL equal to 135 LSB and the DDEM uses P = 128.

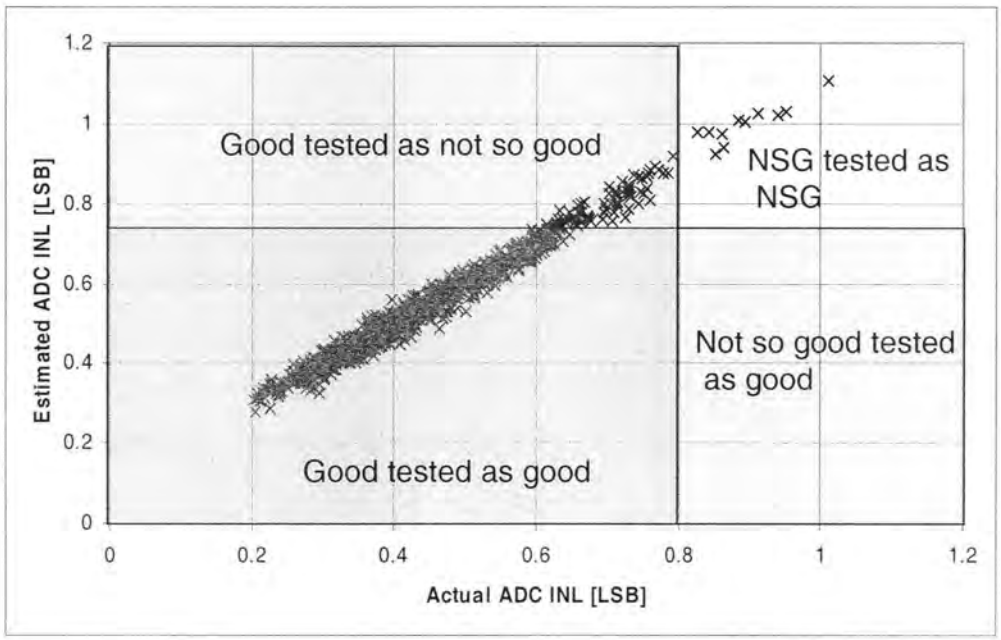


Figure 12: Testing scheme for 1000 ADCs when using a DDEM DAC with P=128

We suppose that those ADCs need to have less than 0.8 LSB INL in order to comply with their specifications, so the testing boundary to say that a part is a good part is below 0.8 LSB. Parts that have INL between 0.8 and 2 LSB are classified as "not so good" (NSG) parts and can be still marketed as less accurate parts. We can see in Figure 12 that although some good parts are tested as not so good ones, there are no NSG parts classified as good ones.

Parts that have INL bigger than 2 LSB are classified as bad parts and should not be shipped to customers. As seen in Figure 13 no bad parts are tested as good ones. It is important to stress that companies do not want to send defective parts to their costumers, which was the case for our method testing.

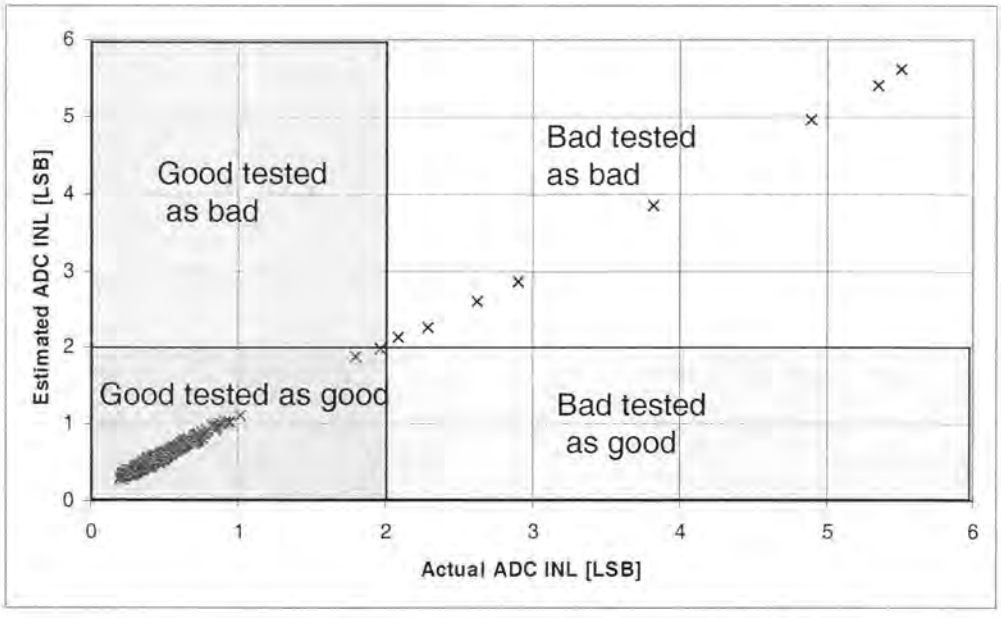


Figure 13: Testing scheme for 1000 ADCs when using a DDEM DAC with P=128

6. Summary

In this paper a deterministic DEM method for testing ADCs is characterized mathematically and also corroborated through simulations. The same method is also compared with a random DEM testing strategy. It was shown by calculations that the DEM approach can significantly improve a DAC signal source's performance in the sense of much improved average linearity. It is also demonstrated that in the DEM testing approach, DACs

that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADCs. In both random and deterministic DEM testing strategies, DEM is not used in the real-time signal path, avoiding some of the limitations related to using DEM for real-time signal processing. Through simulations, it was observed that the performance of the deterministic DEM method is substantially better than what is attainable with a standard random DEM approach from a testing viewpoint. Since the DDEM does not use a randomizer which by itself is a great challenge even at reasonable resolution level, the DDEM method can be used for testing high resolution ADCs. In simulation, the DDEM method is dramatically faster than the random DEM methods, allowing simulation at the 16-18 bit level to be performed at ease. Furthermore, the DDEM method can achieve the same level of testing performance with much smaller number of samples for averaging. The DDEM technique offers potential for use both in BIST and production test environments, since the linearity of the testing signal generator is relaxed and the area required to implement it in silicon is small.

We will extend this work to different DAC and ADC structures and also to different performance parameters that need to be tested for ADCs. There is an actual need in implementing the DDEM DAC with architectures other than thermometer coded structure, since an 18 bit thermometer coded current steering DAC is not feasible. We believe that this problem can be solved. For example, the segmented DAC architecture can be a good alternative choice. Such alternatives are currently under investigation.

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CHAPTER 5: A DETERMINISTIC DYNAMIC ELEMENT MATCHING APPROACH FOR TESTING HIGH RESOLUTION ADCS USING A SEGMENTED THERMOMETER CODED DAC

A paper to be submitted to IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing

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Abstract

Dynamic element matching (DEM) is an effective way to achieve good average performance in the presence of device mismatch, yet it has not been widely adopted because of the time-local stationarity of the signal path. This paper presents a DEM approach to ADC testing in which low precision DEM DACs are used to generate stimulus signals for the ADCs under test. A deterministic DEM (DDEM) switching scheme is applied to a segmented thermometer coded DAC architecture. Detailed simulation results are presented to verify the expected performance of the proposed testing approach. It is demonstrated that the new architecture is able to accurately test ADCs with linearity that exceeds that of the DAC used as the signal generator. The new architecture is suitable for production test and built-in self-test (BIST) environments where high linearity ADCs are difficult to test and characterize.

1. Introduction

Due to increasing resolution and conversion rates, the challenge and cost of testing analog to digital converters (ADCs) is growing. Testing techniques that facilitate a reduction in the cost of test would have a significant impact.

Built-in-self-test (BIST) structures offer the potential to reduce cost while also adding value to the circuits under test. BIST schemes can be used for self-calibration [3] and hence improve circuit performance. Most existing approaches have been aimed at duplicating a

standard tester on chip [4] [5], in other words, to produce a highly accurate and linear stimulus on the chip. However, the prior arts have not demonstrated linearity adequate for testing high resolution ADCs.

The new approach relaxes the linearity requirements on the signal generator and uses signal processing techniques to accurately characterize the device under test (DUT). In [6], the proposed algorithm explores the spatial frequency separation of the nonlinear input from the DUT to characterize the ADC to accuracies that exceeds the linearity of the stimulus. The mathematics behind linearity testing of ADCs using non-linear signals was presented in [7]; where a nonlinear stationary excitation and its shifted replica are needed. In [8] a more rigorous analysis of the methods actually used and the new approach was done by the authors; simulation and experimental results are included.

In this paper dynamic element matching (DEM) is applied to low linearity DACs so that they can be used to test highly-linear ADCs.

Due to process variation, element matching errors are inevitable. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The DEM technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average all element values are nearly equal. The DEM method was used by H. T. Jensen and I. Galton [9] [10] to improve the effective specifications of linearity performance of DACs. It has been demonstrated that DEM can be used to appreciably improve the SFDR performance of moderately low-linearity DACs [9]. Other researchers use DEM in Delta-Sigma Converters. Adams and his colleagues applied DEM in oversampling DACs using noise shaped scramblers to achieve high SNR [11]. Z. Li and T. S. Fiez have studied different DEM algorithms in [12]. A new algorithm is introduced and analyzed on [13] by R. T. Baird and T. S. Fiez. A $\Sigma\Delta$ DAC is implemented using a new algorithm in the work by R. E. Radke, A. Eshraghi and T. S. Fiez [14]. All of these rely on the random nature of DEM to enhance performance.

Our application allows the signal generator to be realized with a low-linearity DAC, eliminating the need of large silicon area and careful design of the test signal generator. A preliminary study investigated the use of random DEM with a highly-nonlinear DAC to test

low-resolution ADCs [15]. The idea behind DEM testing is to generate the ADC stimulus with more than one DAC output sample for a given DAC input digital word; each sample picks different elements following the DEM philosophy. Since DEM is used in the input signal generator we do not have to worry about DEM in the signal path. Deterministic DEM was introduced and compared with the random DEM testing in [16]. It was shown that the DDEM significantly outperformed RDEM. The DDEM method is applied in [17] to a thermometer-coded current steering DAC architecture which is mathematically characterized and verified through simulations. The results show that an 18 bit DAC with 11 bit linearity can be used to characterize a 16 bit linear ADC with an INL error of less than ½ LSB. As an added benefit, the circuit complexity is reduced because no randomizer is required. However, due to the large number of current sources and switching logic, building an on-chip 18 bit linear DAC is impractical. The design is not trivial and a large area is required. A simpler DAC architecture that maintains the benefits of the DAC presented in [17] needs to be developed.

Relaxing the DAC linearity specification reduces the area requirements and simplifies the design effort. A segmented architecture was chosen. Each array (MSB and LSB) will use DDEM as in [17], as explained later in this work.

This paper is organized as follows. An explanation of how the ADC models are implemented and how INL is calculated is given in Section 2. Details are presented in Section 3 about the DDEM segmented thermometer coded DAC architecture, along with mathematical derivation and algorithm description while in Section 4 simulation results for high resolution ADCs are shown and discussed. Section 5 summarizes present and future work in this area.

2. ADC Model and INL calculation

The proposed DEM method for generating stimulus signals can be used for histogram testing of any type of ADC. In the bulk of this paper the focus is on testing flash ADCs, but we will also show results for a pipelined ADC. The method relies only on the transition points of the ADC and hence can be applied to any ADC architecture.

Our flash ADC model assumes resistors mismatch is Gaussian distributed. Non-idealities included in the pipelined ADC model are ADC reference voltage error, ADC interstage amplifier gain error, a open loop DC gain nonlinearity and a capacitance ratio error. All of these factors contribute to the ADC INL.

In the standard histogram test, a linear ramp signal is presented to the input of the ADC. The ADC takes samples of the input and the converted output codes are tallied into corresponding bins. Since V_{in} is proportional to time and the sampling interval is constant, the total number of accumulated samples is proportional to V_{in} and a transition voltage is proportional to the total code hits for all output codes corresponding to lower voltages.

Transition points of an ideal linear ADC are usually called endpoint-fit line transition points and notated as I_k.

$$I_k = T_0 + \frac{T_{N-2} - T_0}{N-2} k, \qquad k = 0,1...N-2 \qquad (1)$$

Equation 1 represents a straight line connecting the first and last transition points of the ADC. Actual transition points of an ADC are compared to corresponding endpoint-fit line transition points for linearity characterization. The difference between the actual transition points and the fit-line transition points is defined as INL and is expressed in LSBs. If we eliminate the dependence on exact values of the first and last transition points, we have

$$INL_k = \frac{T_k - I_k}{1LSB} = \frac{T_k - T_0}{T_{N-2} - T_0}(N-2) - k \qquad (2)$$
$$k = 1,2...N-3$$

By definition, the INL for the first and last transition points are 0 and they don't appear in equation 2.

Naturally, in order for this method to work, it is imperative to have a highly linear ramp input, which can be troublesome when the DUT is a high-resolution ADC. This paper presents methods to overcome this requirement by allowing the use of low linearity DACs to generate a highly linear average input.

3. Dynamic element matching testing

In order to construct a DAC with dynamic element matching, different approaches can be found in the literature [9-14]. RDEM and DDEM were simulated and compared in [16].

In [17], DDEM was formally introduced and characterized for a thermometer coded current steering (TC) DAC structure. As was pointed out on that work the feasibility of such structure for high order DACs was not good since the switching and the number of current sources grow exponentially with the number of bits.

In this paper we introduce a segmented thermometer coded (STC) DAC to reduce the switching and the number of current sources needed on the DAC design while still maintaining the performance of the TC DAC. In [17] it was shown how the DDEM TC DAC could successfully characterize 16 bit linear ADCs with INL errors less than ½ LSB when using a 18 bit resolution effective 11 bit linear DAC. It was also shown that the DAC could be used on a BIST scheme having errors as big as -0.6 LSB. The new structure will be described and characterized mathematically in the succeeding sections.

3.1 Description of DDEM method for STC DAC

In this section we will describe how we apply DDEM to a STC DAC. First we will review the DDEM switching scheme as used in [17] on a thermometer coded current steering DAC. To perform the DDEM method, we add one more current source element to the DAC, so that now the DAC has totally $N = 2^n$ current sources. We use $i_j \quad (j = 1,...,N)$ to represent the j^{th} current source element out of the total N elements, and P represents the number of samples to be generated for each DAC input word. All current sources are arranged conceptually along a circle to visualize the wrapping effect (physical layout of the current sources can be a rectangular array). P starting places that are $q = N / P$ current sources apart are selected. Then, for each input code k, the DAC generates P samples of output where each sample is obtained by switching k current sources consecutively starting from one of the P starting places. The d^{th} $(1 \le d \le P)$ sample is obtained by switching k

current sources starting from $i_{(d-1)q+1}$ in the clock-wise direction. The output analog signal is obtained by forcing the summation of the selected k current sources to drive a resistor R_F.

For an n bit current steering DAC, we can divide the n bits to two parts: $n= n_M+n_L$, where n_M represents the more significant bits and n_L represents the less significant bits. If we let $N_M = 2^{n_M}$ and $N_L = 2^{n_L}$, we have $N = 2^n = N_M \cdot N_L$. For a DAC input code k, we can break it up as following:

$$k = k_M N_L + k_L \begin{pmatrix} 0 \le k \le N-1, \\ 0 \le k_M \le N_M - 1, \\ 0 \le k_L \le N_L - 1 \end{pmatrix} \qquad (3)$$

To get the analog signal corresponding to k, we can obtain the analog signals corresponding to k_M and k_L with different weight respectively first and then combine them together. To implement this, we can use a MSB current source array to generate k_M and use a LSB current source array to generate k_L. Here the MSB and LSB array have N_M-1 and N_L-1 current source elements respectively, and the weight of each MSB array element is N_L times that of a LSB array element. A 4-bit STC current steering DAC is shown in Figure 1 as an example. In this example, n=4, $n_M=n_L=2$ and $N_M=N_L=4$.

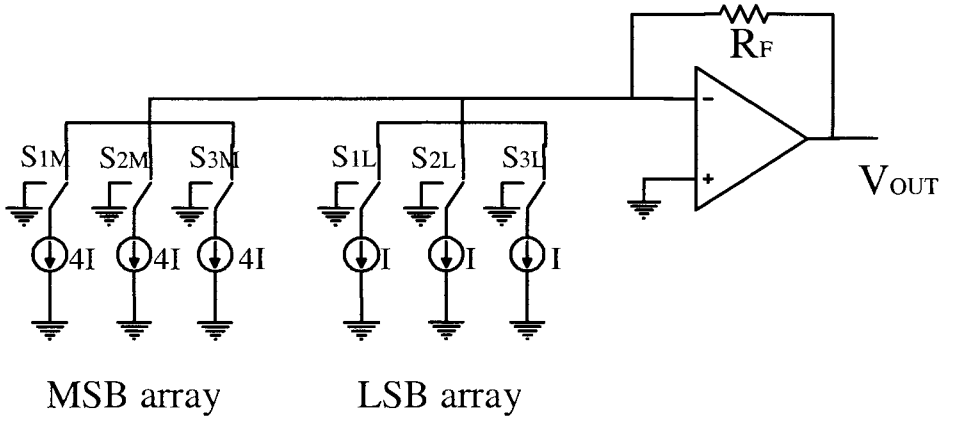
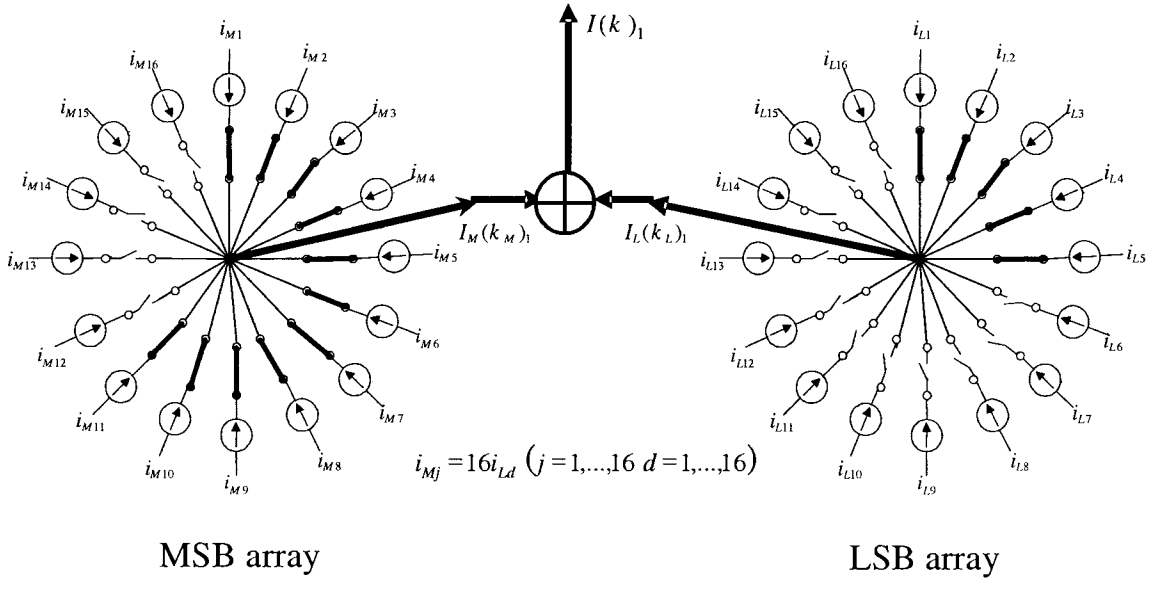


Figure 1: A 4-bit segment coded current steering DAC structure

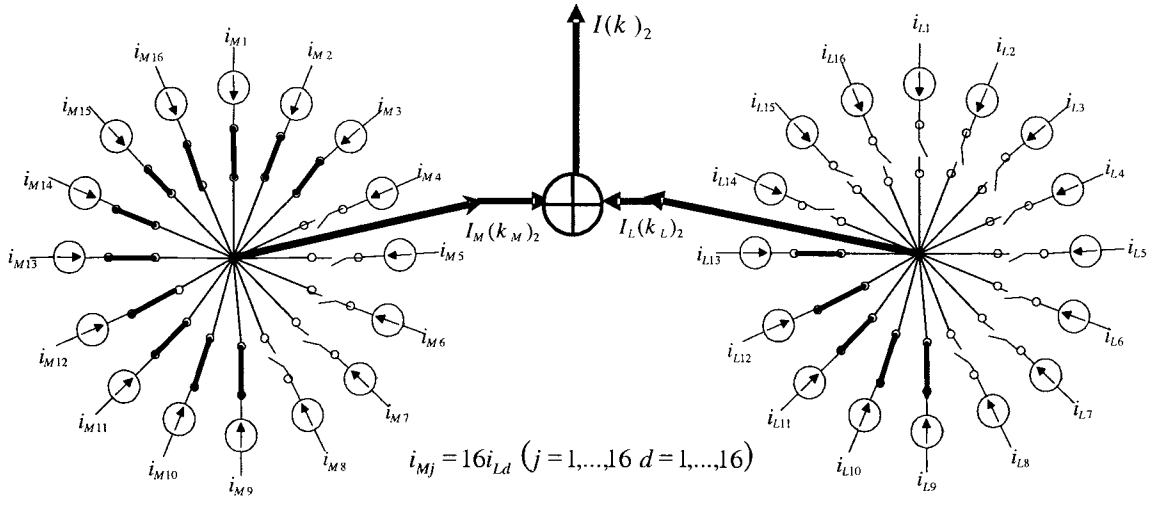
To implement the DDEM [17] for a STC DAC, we only need to apply DDEM to both the MSB array and the LSB array simultaneously. We add one extra current source element for both the MSB and LSB array, then the MSB array has N_M current source elements and

the LSB array has N_L currents source elements. Suppose now that the DAC input code is $k = k_M N_L + k_L$ and that each code needs to have P output samples; then, in order to generate each output sample for a code k, the DDEM method picks k_M current sources from the MSB array and k_L current sources from the LSB array by applying DDEM switching scheme to the MSB and LSB array respectively. Figure 2 illustrates the current source switching scheme for 8-bit STC DAC. In this example we have $n_L=n_M=4$ and $N_L=N_M=16$. For each input code k, 2 samples are output. In Figure 2, $k=191=11\times N_L+5$, hence $k_M=11$ and $k_L=5$. For the 1st output sample, i_{M1}~i_{M11} are selected from the MSB array and i_{L1}~i_{L5} are selected from the LSB array; for the 2nd output sample, i_{M9}~i_{M16}, i_{M1}~i_{M3} are selected from the MSB array and i_{L9}~i_{L13} are selected from the LSB array.



(a)1st output when D=191

Figure 2: DDEM switching of a 8-bit STC DAC



(b) 2nd output when D=191

Figure 2 (continued): DDEM switching of a 8-bit STC DAC

We use $i_{M,j}\ \ (j = 1,..., N_M)$ to represent the j[th] current source element out of the total N_M elements of the MSB array and $i_{L,j}\ \ (j = 1,..., N_L)$ to represent the j[th] current source element out of the total N_L elements of the LSB array. Each DAC input code k has P output samples. Let define $q_M = N_M / P$ and $q_L = N_L / P$. Each output for a given k is just the summation of the selected k_M MSB current elements and k_L LSB current elements. The d[th] current summation is denoted by $I_d(k)$. We have

$$I_d(k) = \sum_{j=1}^{k_M} i_{M,(d-1)q_M + j} + \sum_{j=1}^{k_L} i_{L,(d-1)q_L + j} \quad d = 1,..., P \qquad (4)$$

The average of P samples is denoted by $\bar{I}(k)$

$$\bar{I}(k) = \frac{1}{P} \sum_{d=1}^{P} \left(\sum_{j=1}^{k_M} i_{M,(d-1)q_M + j} + \sum_{j=1}^{k_L} i_{L,(d-1)q_L + j} \right) \qquad (5)$$

Like what we have done to the TC DAC [17], the static performance of the segment coded DAC with DDEM will also be evaluated based on $I_d(k)$ and $\bar{I}(k)$.

3.2 Performance evaluation of the STC DAC with DDEM

In this subsection, we show that the "averaged DAC" of a STC DAC using DDEM approach has a DC transfer curve that approaches a straight line, or equivalently we show that the INL of the averaged DAC is very small. We will also show that the performance degradation due to the segmented structure is limited to an acceptable range.

For the STC DAC, we suppose the desired value for all the MSB array elements is i_{M0} while the desired value for all the LSB array elements is i_{L0}. Due to process and other variations, the actual value of each current source is actually given by:

$$\begin{aligned} i_{M,j} &= i_{M0}(1+\varepsilon_{M,j}) \quad (j=1,...,N_M) \\ i_{L,j} &= i_{L0}(1+\varepsilon_{L,j}) \quad (j=1,...,N_L) \end{aligned} \tag{6}$$

We assume that each MSB array element is just the combination of N_L current source elements that are used to build the TC DAC in [17], and that the LSB array elements are identical to the current source elements used in the TC DAC. Then ideally, $i_{M0}=N_L * i_{L0}$ and then, each $\varepsilon_{M,j}\,(j=1,...,N_M)$ is independent and has an identical Gaussian distribution.

$$\varepsilon_{M,j} \;\; i.i.d. \sim N\left(0, \frac{1}{N_L}\sigma^2\right) \tag{7}$$

The standard deviation of each LSB array element is still σ^2. However, by careful layout design and good matching technique, we can make the relative error between the LSB array element and MSB array elements quite small, and then we can approximate to the following equations:

$$\sum_{j=1}^{N_L} i_{L,j} = \frac{1}{N_M}\sum_{j=1}^{N_M} i_{M,j} \tag{8}$$

$$\sum_{j=1}^{N_L} \varepsilon_{L,j} = \frac{N_L}{N_M}\sum_{j=1}^{N_M} \varepsilon_{M,j} \tag{9.a}$$

If we can make better matching, we can even have

$$\sum_{d=1}^{P} \varepsilon_{L,(d-1)q_L+j} = \frac{N_L}{q_L N_M}\sum_{j=1}^{N_M} \varepsilon_{M,j} \tag{9.b}$$

$$where\; N_L = P \cdot q_L \;\&\; q_L is\; small$$

For the DDEM STC DAC we can use the output current instead of voltage in all of our computations, since R_F is a constant factor and then can be take out of the derivations. We define the fit line based on the two code end points: 0 and N. The corresponding output for the input code 0 for the STC DAC is 0. We assume the output current for input code N is obtained when all the N_M MSB current sources are switched, and it is given by

$$I(N) = \sum_{j=1}^{N_M} i_{M,j} = N_M i_{M0} + i_{M0} \sum_{j=1}^{N_M} \varepsilon_{M,j} \qquad (10)$$

Then the LSB of the DEM segment coded DAC is given by:

$$\overline{LSB} = \frac{I(N)}{N} = \frac{N_M i_{M,0}}{N} + i_{M,0} \frac{1}{N} \sum_{j=1}^{N_M} \varepsilon_{M,j} = i_{L,0} + i_{L,0} \frac{1}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j} \quad (11)$$

It can be verified that $\frac{1}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j}$ is Gaussian and

$$\frac{1}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j} \sim N(0, \frac{1}{N} \sigma^2) \qquad (12)$$

The fit-line of the DEM DAC is then given by:

$$\bar{I}_{fit}(k) = k \cdot \overline{LSB} = k i_{L0} + i_{L0} \frac{k}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j} \quad (13)$$

Based on the fit line, we now compute the INL of the DDEM STC DAC. When the input code is $k = k_M N_L + k_L$, where $k_M = t_M q_M + s_M$ and $k_L = t_L q_L + s_L$, the averaged DAC output current for code k is given by

$$\bar{I}(k) = k \cdot i_{L0} + i_{M0} \cdot \frac{1}{P} \cdot \left(t_M \cdot \sum_{j=1}^{N_M} \varepsilon_{M,j} + \cdot \sum_{d=1}^{P} \sum_{j=1}^{s_M} \varepsilon_{M,(d-1)q_M + j} \right) +$$
$$+ i_{L0} \cdot \frac{1}{P} \cdot \left(t_L \cdot \sum_{j=1}^{N_L} \varepsilon_{L,j} + \cdot \sum_{d=1}^{P} \sum_{j=1}^{s_L} \varepsilon_{L,(d-1)q_L + j} \right) \qquad (14)$$

Subtracting it by the corresponding fit line point yields

$$\overline{INL}(k) = \bar{I}(k) - \bar{I}_{fit}(k)$$

$$= i_{M0} \cdot \frac{1}{P} \cdot \left(t_M \cdot \sum_{j=1}^{N_M} \varepsilon_{M,j} + \cdot \sum_{d=1}^{P} \sum_{j=1}^{s_M} \varepsilon_{M,(d-1)q_M+j} \right) +$$

$$+ i_{L0} \cdot \frac{1}{P} \cdot \left(t_L \cdot \sum_{j=1}^{N_L} \varepsilon_{L,j} + \cdot \sum_{d=1}^{P} \sum_{j=1}^{s_L} \varepsilon_{L,(d-1)q_L+j} \right) - i_{L0} \frac{k}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j}$$

$$= i_{L0} N_L \left[\left(\frac{1}{P} - \frac{s_M}{N_M} \right) \sum_{d=1}^{P} \sum_{j=1}^{s_M} \varepsilon_{M,(d-1)q_M+j} - \frac{s_M}{N_M} \sum_{d=1}^{P} \sum_{j=s_M+1}^{q_M} \varepsilon_{M,(d-1)q_M+j} \right] \quad (15)$$

$$+ i_{L0} \left[\frac{1}{P} \cdot \left(t_L \cdot \sum_{j=1}^{N_L} \varepsilon_{L,j} + \cdot \sum_{d=1}^{P} \sum_{j=1}^{s_L} \varepsilon_{L,(d-1)q_L+j} \right) - \frac{k_L}{N_M} \sum_{j=1}^{N_M} \varepsilon_{M,j} \right]$$

If we apply (9.a) (9.b) to (15), the second part in (15) is equal to 0.

The distribution of the normalized $\overline{INL(k)}$ is then given by:

$$\frac{\overline{INL}\,(k)}{i_{L0}} \sim N\left(0, A\sigma^2\right)$$

$$\textit{where} \qquad A = N_L^2 \left[\left(\frac{1}{P} - \frac{S_M}{N_M} \right)^2 P s_M \frac{1}{N_L} + \left(\frac{S_M}{N_M} \right)^2 P(q_M - s_M) \frac{1}{N_L} \right] = \quad (16)$$

$$= N_L \frac{s_M (q_M - s_M)^2}{P q_M}$$

Note equation (16) is valid only when the MSB array and LSB array are well matched. The variance of $\overline{INL(k)}$ may be larger than expressed in (15) due to the mismatch.

From equation (16), we can also estimate where and how much we expected the maximum deviation from the fit line to be. The variance of $\overline{INL(k)}$ reaches its maximum value at $s_M = \frac{1}{2} q_M$. Using this value for s_M and i_{L0} as 1 LSB, the largest standard deviation of $\overline{INL(k)}$ is

$$\sqrt{N_L \frac{q_M}{4P}}\sigma = \sqrt{\frac{N}{4P^2}}\sigma \quad (17)$$

Comparing with the result obtained for a TC DAC in [17], we find that the result obtained here agrees with (17). Thus, if the MSB and LSB arrays match, the STC structure achieves the same performance as the TC structure. The benefit is that the circuit complexity

is greatly reduced, since fewer current sources and switches are required to implement DDEM. For example, an 18 bit TC DAC requires more than 250.000 current sources, switches, and switch control logic while an 18 bit STC DAC with $N_M = N_L$ needs only 1024. The switching complexity is also reduced considerably, having only to control 512 switches on each array rather than 250,000. To ensure LSB and MSB matching a calibration scheme can be employed to adjust the LSB array values before the DAC is used.

4. DDEM testing simulation results using a STC DAC.

The previous results were validated by simulation. For the following simulation results, the ADCs have 16 bit resolutions while the STC DACs have 18 bits of resolution. All devices were simulated with errors in the ADC's models and in the DAC's current sources. Noise was also added to the DAC output, this noise could be as big as $\pm$ 3 LSB_{DAC}. Also a 1% matching error between the LSB and the MSB arrays was included.

Figure 3 shows the INL distribution of the 1000 simulated flash ADCs. Using a STC DAC with an INL equal to 38 LSB, which means that the actual DAC linearity is less than 12 bits, we estimate the INL for each ADC and calculate how much it deviates from the real ADC INL. The results are shown in Figure 4.

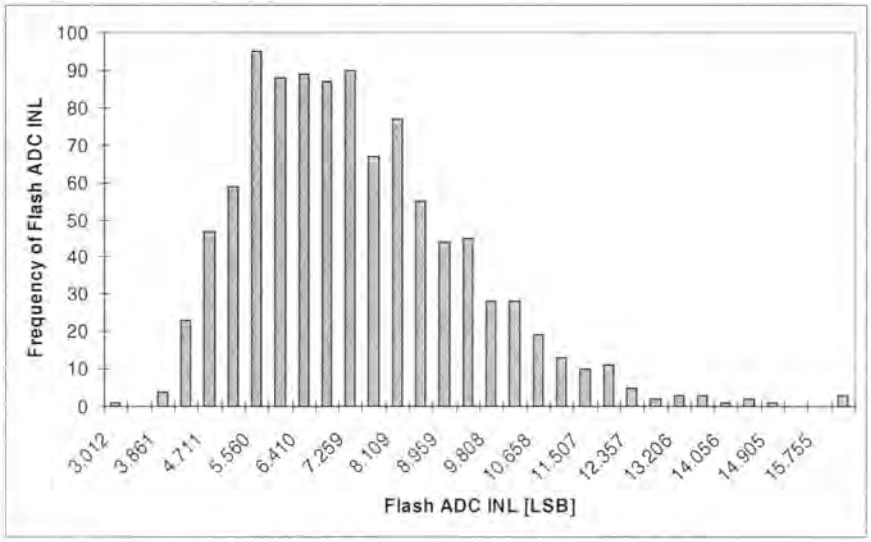


Figure 3: INL distribution for 1000 flash ADCs.

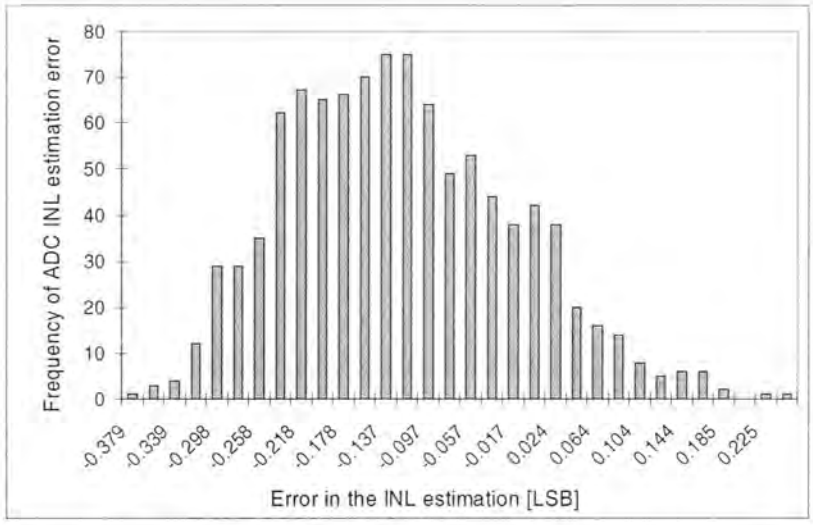


Figure 4: INL estimation error distribution using a DDEM STC DAC to test flash ADCs.

The same test was run using pipelined ADCs, Figures 5 and 6 show the ADC's INL distribution and the error in the estimation respectively.

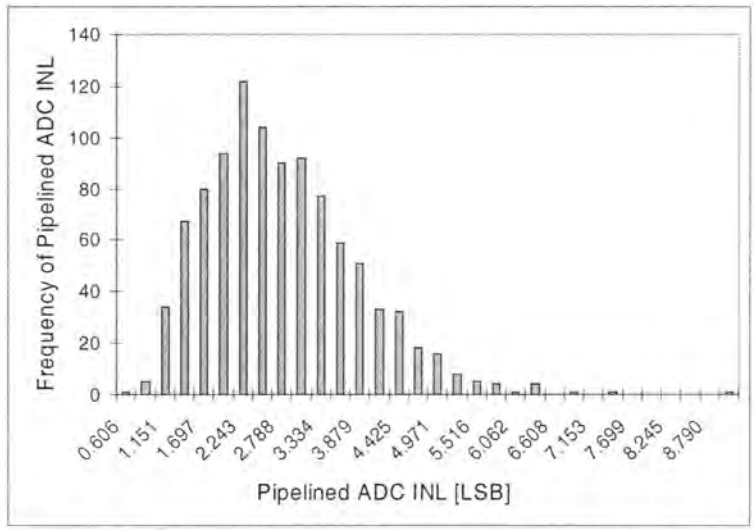


Figure 5: INL distribution for 1000 pipelined ADCs.

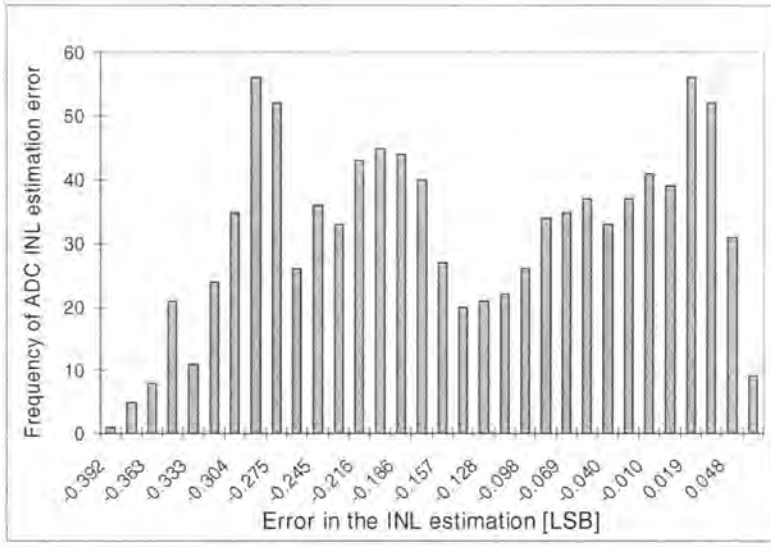


Figure 6: INL estimation error distribution using a DDEM STC DAC to test pipelined ADCs.

Based on these results, the DDEM STC DAC achieves results similar to the TC DAC analyzed in [17]; where the same flash ADCs were tested. The error in the INL estimation using a DDEM TC DAC was between ± 0.2 LSB while when using the DDEM STC DAC is between -0.39 and 0.2 LSB. The degradation in performance may be attributable to LSB and MSB matching error. The degradation in estimation is only a factor of 2 while the area and complexity was significantly reduced. Additionally, INL estimates can be obtained with similar errors for two completely different architectures with different INL values; which says that the test depends on the DAC and not on the ADC architecture or resolution.

The resultant structure is suitable for BIST applications. In that case each ADC has a particular DAC to test it. Figure 7 shows 1000 pairs DAC-ADC; the DAC have the same errors as before, while the flash ADCs used have a INL distribution as shown in Figure 8. As can be seen the ADCs to be tested are actually 16 bit linear since their INL is not bigger than ½ LSB in most of the cases.

We can see that the estimated INL has an error of less than ½ LSB for a majority of the cases, the DACs used for the testing have linearities of 12 to 13 bits without DDEM, which is actually 3 bits less that the linearity of the DUT. This test verifies that the technique is suitable for BIST applications.

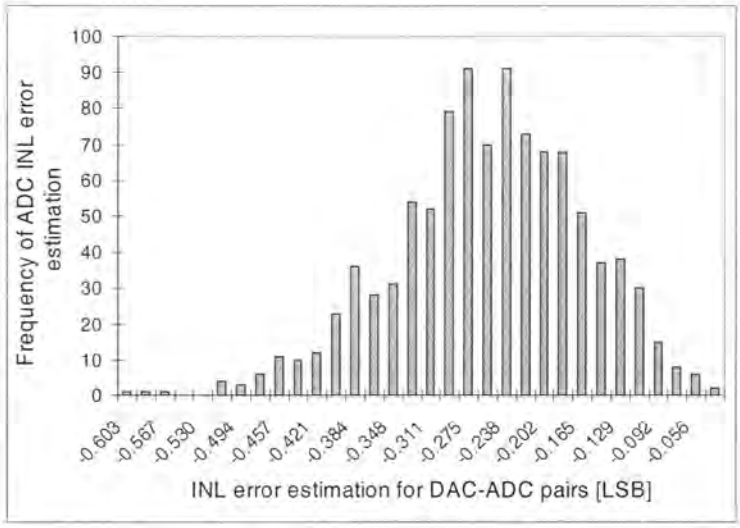


Figure 7: INL error estimation for DDEM STC DAC and flash ADCs 1000 pairs.

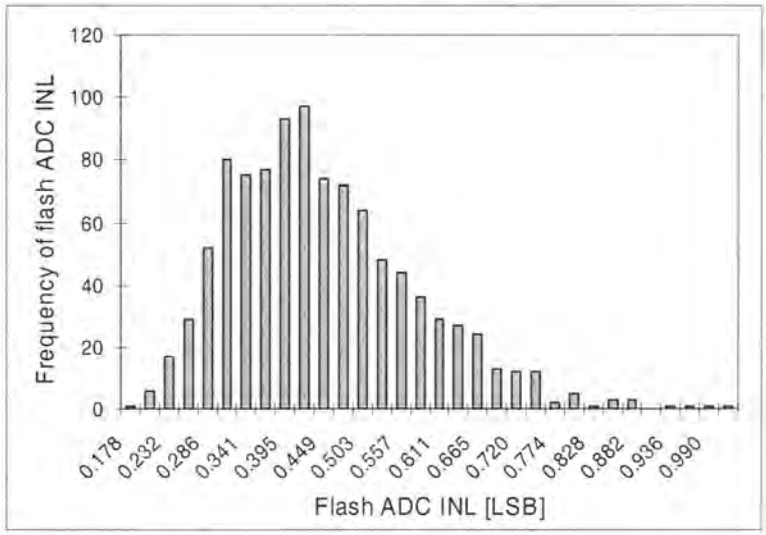


Figure 8: INL distribution for 1000 accurate ADCs.

To verify the performance of the proposed technique as a test tool we simulated 1000 ADCs with INL around 0.5 LSB (Figure 8). The DAC use to estimate the ADCs' INLs has an INL equal to 38 LSB and P = 128.

Assume that the ADCs need to have less than 0.8 LSB INL in order to comply with their specifications, so the testing boundary to say that a part is a good part is below 0.8 LSB. The parts that have INL between 0.8 and 2 LSB are classified as "not so good" (NSG) parts

and can be still marketed as less accurate parts. We can see in Figure 9 that although some good parts are tested as NSG ones, there are no NSG parts classified as good ones, which means that the customer will not receive a deficient part.

If we compare these results with the ones shown in [17] we can see that the TC DAC has a more narrow and centered response, where only 60 good ADCs are categorized as NSG. The STC DAC shown in Figure 9 gives always an overestimation of the INL when the ADC INL is small as in this case, hence 244 good ADCs are cataloged as NSG.

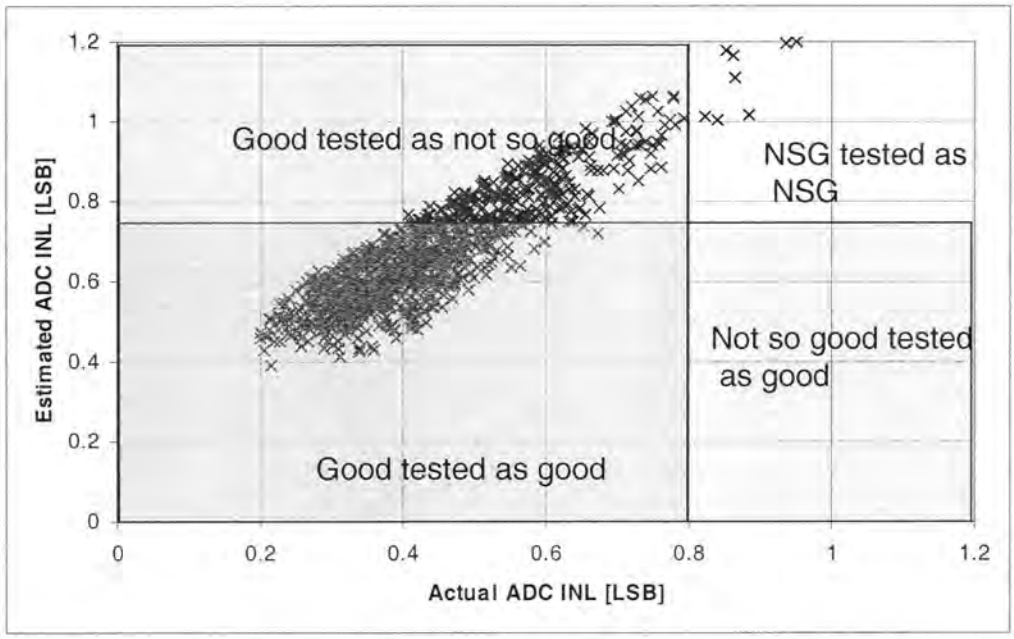


Figure 9: DDEM STC DAC used as a production tester for 1000 accurate flash ADCs.

5. Summary

Simulations were used to validate a new DDEM architecture for testing ADCs. The architecture is more suitable for BIST applications because it requires less area and uses a simpler switching scheme. In the presence of accurate matching or calibration, the performance of the new DDEM STC DAC is similar to the one using a DDEM TC DAC. Simulations show that even in the presence of a small mismatch, the new DDEM STC DAC can be successfully employed.

Two very different ADC architectures were modeled and tested. Simulations show that the method is ADC architecture independent, since it only uses the transition points of the ADC. Future work includes the fabrication of one DDEM STC DAC for testing on silicon.

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CHAPTER 6: GENERAL CONCLUSIONS

A new method for testing ADCs has been introduced. This method is based upon using dynamic element matching (DEM) in signal sources to obtain precise average signal integrity with highly inaccurate sources. Two fundamental variants of this approach have been discussed. One uses a standard dynamic element matching technique in which a randomizer is used to obtain good average performance from matching-critical elements. The second uses deterministic dynamic element matching (DDEM) in which the switching sequence of the matching-critical elements is judiciously selected to achieve nearly perfect average performance. The latter approach requires much shorter switching sequences to obtain a given level of performance and also offers potential for more practical physical implementations. Both techniques are applicable in both production test and BIST environments.

Since the DEM approach is highly tolerant to mismatch in what are normally considered matching-critical components, signal sources can be designed with very small or even minimum-sized devices. In addition to the obvious area savings associated with using small devices, the small device sizes offer potential for operating at much higher speeds since the parasitic capacitances are inherently reduced. The small area requirements make this approach particularly attractive for BIST applications where the on-chip area overhead for any built-in testing circuitry is of considerable concern.

Conventional approaches to testing of ADCs generally require DAC signal sources that have several more bits of resolution than that of the DUT. It has been shown that with the DEM approach, the resolution of the DAC can be comparable to that of the DUT. This offers additional advantages when used in a BIST environment and offers potential for reducing the number of test codes required in a production test environment.

All results presented in this thesis are based on either theoretical formulations or on simulation results. Validation of these concepts in silicon is important and efforts are ongoing to obtain experimental results. The layout of a DDEM DAC designed for 16-bit resolution has been completed in an AMI 0.5μ process.

Statistical characterization of test procedures for DDEM approaches so test boundaries can be established for accurately predicting overall yield of parts shipped to customers are necessary. Future work needs to be carried out in this area.

This work focused on the introduction of the basic concept of using DEM techniques for testing and further work is needed to make these concepts useful to industry. Different DAC architectures and switching schemes need to be investigated so that the most practical approaches can be obtained.